List of Claims

1 (Currently amended) ~~An apparatus that comprises the functions of a conventional random access memory of: (A) means for storing and retrieving data using addressable registers within the apparatus, (B) a plurality of external bus connection to an external bus comprising address bus, data bus and control bus, and (C) the external bus connection facilitating the means for exclusively storing or retrieving data using the addressable registers within the apparatus; wherein the improvement comprising~~ An apparatus of Claim 8, wherein

a) said input/output control unit further comprises a command bit input; and

b) said instruction means further comprises memory means for behaving as a conventional random access memory of said addressable registers when ~~the~~ said command bit input is negatively asserted.

~~c) instruction means for receiving instructions to the apparatus from the external bus when the command bit input is positively asserted~~

2 (Currently amended) Steps for use said apparatus of Claim 8 to store and process array, ~~An apparatus of claim 1, its instruction means~~ further comprising:

~~(a) characterizing means for characterizing the content of multiple internal registers using: (A) the address bus of the external bus to send the characterizing instruction to the apparatus, and (B) the data bus of the external bus to get the characterization result form the apparatus; and~~

~~(b) processing means for concurrently processing multiple internal registers within the apparatus using the address bus or the data bus or both of the external bus to send the processing instruction to the apparatus.~~

a) steps for storing each array item ether (1) in each memory element, or in each fixed number of neighboring memory elements;

b) steps for concurrently defining an new array within an existing array; and

c) steps for concurrently performing a same operation on all array items of said array.

3 (Currently amended) An apparatus of Claim ~~1~~8, wherein said result means further ~~comprising~~ comprises termination means for signaling the termination of ~~the~~ said instruction means by:

a) means for changing the content of ~~the~~ said external bus ~~of the apparatus~~ in a predefined way, or

b) means for waiting a predefined time period before able to receive another input from ~~the~~ said external bus connection, or

c) the combination of (a) and (b).

4 (Currently amended) ~~Compliance means for making the connection to the external bus of the apparatus of Claim 1 in full compliance with a bus standard, the compliance means further comprising:~~ An apparatus of Claim 1, wherein said communication means further comprises compliance means for communicating with a bus stand at said external bus, said compliance means further comprising:

a) means for connecting with said bus standard comprising (1) address bus, (2) data bus and (3) control bus;
b) means for making ~~the apparatus'~~ said external bus connection to ~~the~~ said data bus in full compliance with ~~the data bus portion of the~~ said bus standard~~, and being connected thereof~~;
c) means for making ~~the apparatus'~~ said external bus connection to ~~the~~ said address bus in full compliance with ~~the corresponding bits of the address bus portion of the~~ said bus standard~~, and being connected thereof~~;
d) means for making ~~the apparatus'~~ said command bit input in full compliance with a bit of ~~the~~ said address bus of ~~the~~ said bus standard ~~which is not used to connect to the apparatus' connections to the address bus, as if the address bus bit of the bus standard is being used as a address bus bit, and being connected thereof~~ in full compliance with said bus standard; and
e) means for making ~~the apparatus'~~ said external bus connection to ~~the~~ said control bus in full compliance with ~~the bits or bits' logic combinations of the control bus portion and the remained unconnected bits of the address bus portion of the~~ said bus standard~~, and being connected thereof~~.

5 (Currently amended) Preferred compliance means as cited in Claim 4, wherein said command bit input connects to ~~the apparatus' connection to the external bus in full compliance with a bus standard as claimed in Claim 4, the preferred compliance means further comprising connecting the apparatus' command bit input with~~ the least significant address bit of ~~the~~ said bus standard ~~which is not connected to the apparatus' external bus connection to the address bus~~.

6 (Cancelled)

7 (Currently amended) ~~Using~~ Steps for using ~~the~~ said apparatus ~~when it is connected with other devices using an external bus of a bus standard,~~ as claimed in ~~Claim 4~~ Claim 1, ~~the using steps~~ further comprising:
a) negatively asserting ~~the~~ said command bit input ~~of the apparatus~~, to use ~~the~~ said apparatus as a conventional random access memory,
b) positively asserting ~~the~~ said command bit input ~~of the apparatus~~, and sending a data processing instruction to ~~the~~ said apparatus as if storing data to a fictional location inside ~~the~~ said apparatus, and
c) positively asserting ~~the~~ said command bit input ~~of the external bus~~, and sending a data characterizing instruction to ~~the~~ said apparatus as if retrieving data from a fictional location inside ~~the~~ said apparatus.

8 (Currently amended) An apparatus comprising:
a) a plurality of memory elements, each of which comprising:
   1) at least one register, comprising at least one addressable register;
   2) an enable bit input;
   ~~3) element instruction means for receiving and carrying out instructions for the memory element;~~

~~4) disabling means for disabling the element instruction means when the enable bit input is negatively asserted;~~

3) an instruction input;

4) execution means for carrying out instructions at said instruction input only when said enable bit is positively asserted;

5) a unique element address;

~~(b) a concurrent bus, which is connected to all the memory elements, and which is concurrently read by all the enabled memory elements;~~

~~(c) an exclusive bus, which is connected to a plurality of registers, and which is exclusively read from or exclusively written to by any one of the connected registers, the connected registers being addressable registers, each having a register address;~~

b) an input/output control unit, comprising:

~~(1) means for connecting with external bus connection of the apparatus, and means for receiving instruction from the external bus;~~

~~(2) means for connecting to the concurrent bus, and means for writing exclusively to the concurrent bus; and~~

~~(3) means for connecting to the exclusive bus, and means for either (A) exclusively writing to the exclusive bus, or (B) exclusively reading from the exclusive bus;~~

1) an external bus connection, and

2) communication means for communicating with said external bus;

c) exclusive means for exclusively copying either (1) the content of any said addressable register to ~~its~~ said external bus connection, or (2) the content of ~~its~~ said external bus connection to any said addressable register~~, or (3) the content of a source within the input/output control unit to the exclusive bus; or (4) the content of the exclusive bus to a target within the input/output control unit~~;

d) concurrent means for concurrently executing a same instruction in one or a plurality of ~~its~~ said enabled memory elements, ~~the~~ said concurrent means further comprising:

1) instructing means for sending ~~an~~ said instruction concurrently~~, through the concurrent bus,~~ to ~~each said memory element~~;

2) enabling means for concurrently positively asserting ~~the~~ said enable bit inputs of ~~a plurality of~~ all said memory elements whose element addresses are (A) no less than a start element address, (B) no more than an end element address, and (C) an integer increment of a carry number starting from said start element address; and

3) executing means for concurrently executing ~~the~~ said instruction in ~~each of~~ all ~~the~~ said enabled memory elements; and

e) instruction means for receiving and carrying out instructions at ~~the~~ said external bus connection, further comprising:

1) command means for translating the content at said external bus connection into said exclusive means and said concurrent means;

2) result means for presenting the execution result of said command means at said external bus connection.

9 (Currently amended) An apparatus of Claim 8, wherein said result ~~its instruction~~ means further ~~comprising~~ comprises means for signaling the current output value of said external bus connection ~~the values of all the outputs of the apparatus~~ being invalid for the current input value of said external bus connection.

~~b) means for translating the content of the external bus of the apparatus into instructions for the apparatus; and~~

~~c) means for carrying out the instruction for the apparatus in a series of steps comprising the concurrent means and the exclusive means.~~

10 (Cancelled)

11 (Currently amended) An apparatus of Claim ~~10~~8, ~~its instruction means~~ further comprising:

a) an instruction kernel; and

b) said command means further comprising means for using said instruction kernel to translate ~~translating~~ the content of ~~its~~ said external bus into instructions for ~~the~~ said apparatus ~~when the command bit input is positively asserted~~.

~~c) means for signaling the values of all the outputs of the apparatus being invalid for the current input values;~~

~~d) means for carrying out the instruction for the apparatus in a series of steps comprising the concurrent means and the exclusive means; and~~

~~e) means for using an existing bus standard protocol to signal the readiness of the apparatus.~~

12 (Currently amended) An apparatus of Claim 8, further comprising:

a) a plurality of bit storage elements;

b) means for connecting each enable bit input of all ~~the~~ said memory elements from a unique bit storage element; and

c) ~~the~~ said enabling means further comprising means for using ~~the~~ said bit storage elements to positively assert each corresponding enable bit input of all ~~the~~ said enabled memory elements, while negatively assert each corresponding enable bit input of all other said memory elements.

13 (Cancelled)

14 (Currently amended) An apparatus of Claim 8, further comprising:

a) a range decoder, comprising:
   1) a start address input;
   2) an end address input;
   3) a plurality of bit outputs, each of which has a unique address; and
   4) means for concurrently positively asserting all ~~the~~ said bit outputs whose addresses are: (A) no less than the value at ~~the~~ said start address input, and (B) no more than the value at ~~the~~ said end address input, while negatively asserting all ~~the~~ other said bit outputs;

b) means for connecting each of all ~~the~~ said memory elements to a unique bit output of ~~the~~ said range decoder wherein the element address of each said memory element equals the corresponding bit output address of said range decoder~~, thus each of all the memory elements having a unique element address~~; and

c) ~~the~~ said enabling means further comprising means for using said range decoder to enable all said memory elements, wherein said carry number is a constant one

~~positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than a start address, and (B) no more than an end address; and~~

~~d) the input/output control unit further comprising controlling means for providing the start address input and the end address input to the range decoder.~~

15 (Currently amended) An apparatus of Claim 8, further comprising:

a) a general decoder, comprising:
   1) a start address input;
   2) an end address input;
   3) a carry number input;
   4) a plurality of bit outputs, each of which has a unique address; and
   5) means for concurrently positively asserting all ~~the~~ said bit outputs whose addresses are: (A) no less than the value at ~~the~~ said start address input, (B) no more than the value at ~~the~~ said end address input, and (C) an integer increment of the value at ~~the~~ said carry number input starting from the value at ~~the~~ said start address input, while negatively asserting all ~~the~~ other said bit outputs;

b) means for connecting each of all ~~the~~ said memory elements to a unique bit output of ~~the~~ said general decoder wherein the element address of each said memory element equals the corresponding bit output address of said general decoder~~, thus each of all the memory elements having a unique element address~~; and

c) ~~the~~ said enabling means further comprising means for using said general decoder to enable all said memory elements. ~~positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than a start address, (B) no more than an end address, and (C) an integer increment of a carry number starting from the start address; and~~

~~d) the input/output control unit further comprising controlling means for providing the start address input, the end address input and the carry number input to the general decoder.~~

16 (Currently amended) An apparatus of Claim 8 ~~15, its general decoder further comprising~~ wherein the value of ~~the~~ said carry number ~~of the carry number input being~~ is no larger than the square root of the total count of said memory elements ~~count of the apparatus~~.

17-26 (Cancelled)

27 (Currently amended) An apparatus ~~of claim 8, each memory element further~~ comprising:

a) a plurality of memory elements, each of which comprising:
   1) at least one register, comprising at least one addressable register;
   2) an enable bit input;
   3) an instruction input;
   4) execution means for carrying out instructions at said instruction input only when said enable bit input is positively asserted;
   5) a match bit output;

6) state means for defining states for ~~the~~ said memory element; and
7) matching means for positively asserting ~~its~~ said match bit output only when ~~the~~ said memory element is in a required state and said enable bit input is positively asserted;
~~1) the disabling means further comprising means for negatively asserting the match bit output when the enable bit input is negatively asserted.~~

b) an input/output control unit, comprising:
1) an external bus connection, and
2) communication means for communicating with said external bus;

c) exclusive means for exclusively copying either (1) the content of any said addressable register to said external bus connection, or (2) the content of said external bus connection to any said addressable register;

d) concurrent means for concurrently executing a same instruction in one or a plural of said memory elements, said concurrent means further comprising:
1) enabling means for concurrently positively asserting said enable bit inputs of all memory elements whose element addresses are (A) no less than a start element address, (B) no more than an end element address, and (C) an integer increment of a carry number starting from said start element address;
2) instructing means for sending said instruction concurrently to all said memory elements;
3) executing means for concurrently executing said instruction in all enabled memory elements;
4) matching request means for using a required state for matching concurrently at all enabled memory elements; and
5) finding means for concurrently finding said memory elements whose match bit outputs have been positively asserted; and

h) instruction means for receiving and carrying out instructions at said external bus connection, further comprising:
1) command means for translating the content at said external bus connection into said exclusive means and said concurrent means;
2) result means for presenting the execution result of said command means at said external bus connection.

28 (Currently amended) An apparatus of claim 27, wherein each of all ~~the~~ said memory elements further ~~comprising~~ comprises:
a) a bit storage element; and
b) ~~saving~~ means for saving the value of ~~the~~ said match bit output in ~~the~~ said bit storage element ~~when the memory element is enabled~~.

29 (Currently amended) An apparatus of claim ~~28~~27, wherein each of all ~~the~~ said memory elements further ~~comprising~~ comprises:
a) neighboring means for reading ~~the saved value of~~ the match bit output of the memory element whose element address is either immediately lower or immediately higher than the element address of ~~the~~ said memory element ~~itself~~;

b) combining means for using ~~the saved value of the~~ said neighboring match bit output ~~of said neighboring memory element~~ in defining ~~the~~ said state of ~~the~~ said memory element ~~itself~~; and
c) transferring means for using ~~the saved value of the~~ said neighboring match bit output ~~of said neighboring memory element~~ as ~~the~~ said state of ~~the~~ said memory element ~~itself~~.

30 (Currently amended) An apparatus of Claim 27, further comprising:
a) a parallel counter, comprising:
1) a plurality of bit inputs,
2) a count output, and
3) means for concurrently counting ~~the~~ said bit inputs which are positively asserted;
b) means for connecting ~~(1) the~~ each match bit output ~~of each~~ of all ~~the~~ said memory elements to a unique bit input of ~~the~~ said parallel counter; and
~~(2) the count output of the parallel counter to the input/output control unit;~~
c) said finding means further comprising counting means for concurrently counting said enabled memory elements whose match bit outputs are positively asserted.
~~(c) the concurrent means further comprising:~~
~~(1) matching means for specifying the required state for matching concurrently to all the memory elements by the data stored in each enabled memory element and a matching requirement; and~~
~~(2) counting means for concurrently counting the enabled memory elements whose match bit outputs are positively asserted; and~~
~~d) the instruction means further comprising:~~
~~(1) means for concurrently specifying a matching requirement to each of all the memory elements; and~~
~~(2) means for writing the count of the enabled memory elements which satisfy the matching requirement to the external connection of the apparatus.~~

31 (Currently amended) Steps for using ~~the~~ said apparatus of Claim 30, further comprising:
a) steps for concurrently defining or concurrently changing the selection of ~~the~~ said enabled memory elements for matching;
~~(b) steps for concurrently specifying a matching requirement to each of all the memory elements; and~~
b) steps for concurrently finding no said enabled memory element satisfying a matching requirement; and
c) steps for concurrently counting ~~the~~ said enabled memory elements each of which ~~satisfies~~ satisfy a matching requirement.

32 (Currently amended) An apparatus of Claim 27, further comprising:
a) a priority encoder, comprising:
1) a plurality of bit inputs, each of which ~~corresponds to~~ has a unique address;
2) a no-hit bit output, which is positively asserted only when none of ~~the~~ said bit inputs is positively asserted;
3) a priority high bit input;

4) an address output, ~~when the no-hit bit output being negatively asserted, the address output~~ which contains ~~containing~~ either (A) the highest address of ~~the~~ said bit inputs which are positively asserted when ~~the~~ said priority high bit input is positively asserted, or (B) the lowest address of ~~the~~ said bit inputs which are positively asserted when ~~the~~ said priority high bit input is negatively asserted;~~ and~~

b) means for connecting ~~(1) the~~ each match bit output of ~~each of~~ all ~~the~~ said memory elements to a unique bit input of ~~the~~ said priority encoder wherein the element address of each said memory element equals the corresponding bit input address of said priority encoder; and~~, thus each of all the memory elements having an address~~;

~~(2) the priority high bit input of the priority encoder from the input/output control unit; and~~

~~(3) the no-hit bit output and the address output of the priority encoder to the input/output control unit;~~

c) said finding means further comprising:

1) means for finding no said enabled memory elements whose match bit outputs are positively asserted; and

2) means for finding either (A) the highest or (B) the lowest element address of said enabled memory elements whose match bit outputs are positively asserted.

~~(c) the concurrent means further comprising:~~

~~(1) matching means for specifying the required state for matching concurrently to all the memory elements by the data stored in each enabled memory element and a matching requirement;~~

~~(2) null means for signaling none of the enabled memory elements whose match bit outputs are positively asserted; and~~

~~(3) addressing means for finding either the highest or the lowest element address of the enabled memory elements whose match bit outputs are positively asserted; and~~

~~(d) the instruction means further comprising:~~

~~(1) means for concurrently specifying a matching requirement to each of all the memory elements;~~

~~(2) means for writing a predefined value to the external connection of the apparatus if no enabled memory element satisfying the matching requirement; and~~

~~(3) means for writing to the external connection of the apparatus either (A) the highest or (B) the lowest address among those of the enabled memory elements which satisfy the matching requirement.~~

33 (Currently amended) Steps for using ~~the~~ said apparatus of Claim 32, further comprising:

a) steps for concurrently defining or concurrently changing the selection of ~~the~~ said enabled memory elements for matching;

~~(b) steps for concurrently specifying a matching requirement to each of all the memory elements;~~

b) steps for concurrently finding ~~none of the~~ no said enabled memory elements ~~which satisfy~~ satisfying a matching requirement;

c) steps for concurrently finding the highest address of ~~all the~~ said enabled memory elements which satisfy a matching requirement;

d) steps for concurrently finding the lowest address of ~~all the~~ said enabled memory elements which satisfy a matching requirement; and
e) steps for enumerating the element addresses of ~~all the~~ said enabled memory elements each of which satisfies a matching requirement.

34 (Currently amended) An apparatus of Claim 32, further comprising:
a) a parallel counter, comprising:
1) a plurality of bit inputs,
2) a count output, and
3) means for concurrently counting ~~the~~ said bit inputs which are positively asserted;
b) means for connecting ~~(1) the~~ said match bit output of each of all ~~the~~ said memory elements to a unique bit input of ~~the~~ said parallel counter; and
~~2) the count output of the parallel counter to the input/output control unit;~~
c) said finding means further comprising counting means for concurrently counting said enabled memory elements whose match bit outputs are positively asserted.
~~(c) the concurrent means further comprising:~~
~~(1)matching means for specifying the required state for matching concurrently to all the memory elements by the data stored in each enabled memory element and a matching requirement; and~~
~~(2) counting means for concurrently counting the enabled memory elements whose match bit outputs are positively asserted; and~~
~~(d) the instruction means further comprising:~~
~~(1) means for concurrently specifying a matching requirement to each of all the memory elements; and~~
~~(2) means for writing the count of the enabled memory elements which satisfy the matching requirement to the external connection of the apparatus.~~

35 (Currently amended) Steps for using ~~the~~ said apparatus of Claim 34, further comprising:
a) steps for concurrently defining or concurrently changing the selection of ~~the~~ said enabled memory elements for matching;
~~(b) steps for concurrently specifying a matching requirement to each of all the memory elements;~~
b) steps for concurrently finding ~~none of the~~ no said enabled memory elements ~~which satisfy~~ satisfying a matching requirement;
c) steps for concurrently finding the highest address of ~~all the~~ said enabled memory elements which satisfy a matching requirement;
d) steps for concurrently finding the lowest address of ~~all the~~ said enabled memory elements which satisfy a matching requirement; and
e) steps for enumerating the element addresses of ~~all the~~ said enabled memory elements each of which satisfies a matching requirement.
f) steps for concurrently counting ~~the~~ said enabled memory elements each of which satisfies a matching requirement.

36 (Currently amended) An apparatus of Claim 34, further comprising:
a) a general decoder, comprising:

1) a start address input;
2) an end address input;
3) a carry number input;
4) a plurality of bit outputs, each of which has a unique address; and
5) means for concurrently positively asserting all ~~the~~ said bit outputs whose addresses are: (A) no less than the value at ~~the~~ said start address input, (B) no more than the value at ~~the~~ said end address input, and (C) an integer increment of the value at ~~the~~ said carry number input starting from the value at ~~the~~ said start address input, while negatively asserting all ~~the~~ other said bit outputs;

b) means for connecting each of all ~~the~~ said memory elements to ~~a unique~~ said bit output of ~~the~~ said general decoder wherein the element address of each said memory element equals the corresponding bit output address of said general decoder;

c) ~~the~~ said enabling means further comprising means for using said general decoder to enable all said memory elements. ~~positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than a start address, (B) no more than an end address, and (C) an integer increment of a carry number starting from the start address; and~~

~~d) the input/output control unit further comprising controlling means for providing the start address input, the end address input, and the carry number input to the general decoder.~~

37 (Currently amended) An apparatus of claim 36, further comprising dividing means for ~~obtaining (A) the quotient and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset~~ dividing a dividend by a divisor to obtain the quotient and the remainder of said division, wherein said dividend equals the value of subtracting an offset from a subtrahend, said ~~the~~ dividing means further comprising:

a) means for inputting ~~the~~ said offset into ~~the~~ said start address input of ~~the~~ said general decoder;

b) means for inputting ~~the~~ said subtrahend to ~~the~~ said end address input of ~~the~~ said general decoder;

c) means for inputting ~~the~~ said divider to ~~the~~ said carry number input of ~~the~~ said general decoder;

d) means for connecting each of all bit outputs of ~~the~~ said general decoder to a unique bit input of ~~the~~ said parallel counter~~, except the bit output at address 0 of the general decoder~~;

e) means for outputting from ~~the~~ said count output of ~~the~~ said parallel counter the value of said quotient plus one;

f) means for connecting each of all bit outputs of ~~the~~ said general decoder to a unique ~~the~~ bit input of ~~the~~ said priority encoder wherein each bit input address of said priority encoder equals the corresponding bit output address of said general decoder ~~which has the same address, except the bit output at address 0 of the general decoder~~;

g) means for positively asserting ~~the~~ said priority high bit input of ~~the~~ said priority encoder;

~~h) when the said no-hit bit output of the said priority encoder is positively asserted, means for signaling the said divider being 0; and~~

h) ~~when the no-hit bit output of the priority encoder is negatively asserted~~, means for outputting the value of said dividend minus said reminder from ~~the~~ said address output of ~~the~~ said priority encoder.~~; and~~

~~i) the instruction means further comprising means for obtaining (1) the quotient, and (2) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset.~~

38 (Currently amended) An apparatus of Claim 37, further comprising:

a) a plurality of bit storage elements;

b) means for connecting:

1) each enable bit input of all ~~the~~ said memory elements from a unique bit storage element; and

2) each of all ~~the~~ said bit storage element from a unique bit output of ~~the~~ said general decoder wherein the element address of each said memory element equals the bit output address of said general decoder;

c) said enabling means further comprising retaining means for retaining the value of ~~the~~ said bit storage elements when obtaining ~~(1) the quotient, and (2) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset~~ the result of said dividing means, so that said enabling means and said dividing means can be carried out concurrently.

39 (Currently amended) An apparatus of claim 27, wherein each of ~~its~~ said memory elements further comprising:

a) at least one status bit;

b) status means for either positively or negatively asserting any of ~~the~~ said status bits, and

c) ~~the~~ said state means further comprising means for using the values of ~~the~~ said status bits to define ~~the~~ said state of ~~the~~ said memory element.

40 (Currently amended) An apparatus of Claim 27, ~~each memory element further comprising the required state being a predefined state~~ wherein said required state of matching of said memory elements is predefined.

41 (Currently amended) An apparatus of Claim 27, ~~further comprising~~ wherein:

a) ~~the concurrent bus further carrying~~ said instruction means further comprises means for sending a condition ~~specification~~ code to ~~each of all the~~ said memory elements; and

b) ~~the~~ said matching means further ~~comprising~~ comprises ~~(1) specifying~~ means for ~~using the~~ translating said condition ~~specification~~ code ~~of the concurrent bus~~ to ~~specify the~~ said required state of matching~~, and (2)determining means for determining if the state of the memory element matches the required state which has been specified by the condition specification of the concurrent bus~~.

42-65 (Cancelled)

66 (Currently amended) An apparatus of Claim 27, ~~further comprising~~ wherein:

~~(a) the concurrent bus further carrying a condition datum to all the memory elements;~~

a) each of ~~its~~ all said memory elements further ~~comprising~~ comprises: ~~comprising means for connecting:~~

~~(1) a register to the first input of the value comparator, the register being called the comparable register of the memory element; and~~

~~(2) the condition datum of the concurrent bus to the second input of the value comparator; and~~

1) only one addressable register;

2) said instruction input further comprising:

A) a datum; and

B) a comparison code, specifying the condition of either (i) equal, or (ii) unequal, or (iii) greater than, or (iv) less than, or (v) greater than or equal, or (vi) less than or equal;

3) a value comparator, comparing said datum and said addressable register, and outputting a comparison result; and

4) said matching means further comprising means for positively asserting said match bit output only when said comparison result meets said comparison code; and

b) ~~its~~ said concurrent means further ~~comprising~~ comprises means for ~~positively asserting the match bit outputs of each of all the enabled memory elements whose comparable registers having value satisfying the comparing requirement of either (A) equal, or (B) unequal, or (C) larger than, or (D) smaller than, or (E) equal or larger than, or (F) equal or smaller than, with the value of the condition datum of the concurrent bus~~ concurrently finding any value match between a value and the content of addressable register of each enabled memory element.

67 (Currently amended) An apparatus of Claim 66, ~~further comprising~~ wherein:

~~(a) the concurrent bus further carrying to each of all the memory elements:~~

~~(1) a condition datum; and~~

~~(2) a mask;~~

a) each of ~~its~~ all said memory elements further ~~comprising~~ comprises:

~~1) a bus AND gate, comprising:~~

~~(A) a first input;~~

~~(B) a second input; and~~

~~(C) a output, each of its bit being positively asserted when the corresponding bits of the first input and the second input are both positively asserted; and~~

~~(2) means for connecting:~~

~~(A) a register to the first input of the bus AND gate, the register being called the comparable register of the memory element;~~

~~(B) the mask of the concurrent bus to the second input of the bus AND gate;~~

~~(C) the output of the bus AND gate to the first input of the value comparator; and~~

~~(D) the condition datum of the concurrent bus to the second input of the value comparator; and~~

1) said instruction input further comprising a mask;

2) means for masking the content of said addressable register with said mask; and

3) means for comparing said masked content of said addressable register with said datum in said value comparator; and

b) ~~its~~ said concurrent means further ~~comprising~~ comprises means for ~~positively asserting the match bit outputs of each of all the enabled memory elements whose comparable registers after being masked by the mask of the concurrent bus having value satisfying the comparing requirement of either (A) equal, or (B) unequal, or (C) larger than, or (D) smaller than, or (E) equal or larger than, or (F) equal or smaller than, with the value of the condition datum of the concurrent bus~~ concurrently finding any value match between a value and said masked content of addressable register of each enabled memory element.

68-69 (Cancelled)

70 (Currently amended) Combined comparing steps for comparing (A) array items stored in ~~the comparable registers of an~~ said apparatus as Claim ~~70~~106, with (B) a value to be compared which has several portions~~, each array item having corresponding multiple portions, with each portion spanning a memory element~~, ~~the~~ said combined comparing steps further comprising:

a) steps for storing each array item by multiple neighboring memory elements in the order of significance, so that each memory element for each array item is identified by a unique significance;

~~b) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for searching;~~

b) steps for concurrently defining an new array within an existing array;

c) step for concurrently positively asserting the ~~shared register of each of all the memory elements whose comparable register holds the most significant portion~~ match bits of all most significant memory element only when said most significant memory element has value that equals the most significant portion of the value to be compared;

d) in the decreased significance from the second most significant memory element to the least significant memory element of each of all array items, steps for concurrently positively asserting the ~~shared register of each of all the memory elements~~ match bit of each memory element only when: (A) ~~the comparable register~~ said memory has value that equals the corresponding portion of the value to be compared; and (B) the neighboring memory element of immediately higher significance of said memory element has positively asserted ~~shared register~~ match bit;

e) steps for using the match bit outputs of all least significant memory element to signal the equal/unequal matching of the array items with the value to be compared;

f) in the increased significance from the least significant memory element to the most significant memory element of each of all array items:

1) steps for concurrently positively asserting the ~~shared register~~ match bit of each ~~of all the~~ memory elements only when (A) ~~the value of the comparable register satisfies the condition code of the concurrent bus~~ said memory element satisfies said comparison matching with the corresponding portion of the value to be compared, and (B) ~~the shared register~~ said match bit ~~of the memory element itself~~ is originally negatively asserted; and

2) steps for concurrently transferring the content of the ~~shared register~~ said match bit of ~~each of all the memory elements~~ from the ~~shared register~~ match bit of the neighboring memory element of immediately lower significance of said memory element only when ~~the shared register of the memory element itself~~ said match bit is originally positively asserted; and

g) steps for using the match bit output of ~~the~~ said most significant memory element of each of all array items to signal the comparison matching of the array items with the value to be compared.

71-72 (Cancelled)

73 (Currently amended) An apparatus of Claim 66, further comprising:

a) a priority encoder, comprising:
   1) a plurality of bit inputs, each of which ~~corresponds to~~ has a unique address;
   2) a no-hit bit output, which is positively asserted only when none of ~~the~~ said bit inputs is positively asserted;
   3) a priority high bit input; and
   4) an address output, ~~when the no-hit bit output being negatively asserted, the address output~~ which containing either (A) the highest address of ~~the~~ said bit inputs which are positively asserted when ~~the~~ said priority high bit input is positively asserted, or (B) the lowest address of ~~the~~ said bit inputs which are positively asserted when ~~the~~ said priority high bit input is negatively asserted; ~~and~~

b) means for connecting ~~(1)~~ the match bit output of each of all ~~the~~ said memory elements to a unique bit input of ~~the~~ said priority encoder wherein the element address of each said memory element equals the corresponding bit input address of said priority encoder; and~~, thus each of all the memory elements having an address~~;
   ~~2) the priority high bit input of the priority encoder from the input/output control unit; and~~
   ~~3) the no-hit bit output and the address output of the priority encoder to the input/output control unit;~~

c) said finding means further comprising:
   1) means for finding no said enabled memory elements whose match bit outputs are positively asserted; and
   2) means for finding either (A) the highest or (B) the lowest element address of said enabled memory elements whose match bit outputs are positively asserted.

~~(c) the concurrent means further comprising:~~
   ~~(1) comparing means for specifying the required state for matching concurrently to all the memory element by the data stored in each enabled memory element and a comparison requirement;~~
   ~~(2) null means for signaling none of the enabled memory elements whose match bit output is positively asserted; and~~
   ~~(3) addressing means for finding either the highest or the lowest element address of the enabled memory element whose match bit output is positively asserted; and~~

~~(d) the instruction means further comprising:~~
   ~~(1) means for concurrently specifying a comparison requirement to each of all the memory elements;~~

~~(2) means for writing a predefined value to the external connections of the apparatus if no enabled memory element satisfying the comparison requirement; and~~

~~(3) means for writing to the external connections of the apparatus either (A) the highest or (B) the lowest address of the enabled memory element which satisfies the comparison requirement.~~

74 (Currently amended) Steps for using said apparatus of Claim 73 to store and manage an array, further comprising:

~~(a) steps for concurrently specifying a comparison requirement to each of all the memory elements;~~

~~(b) steps for storing an array by the apparatus;~~

a) steps for storing each array item either (1) in each memory element or (2) in each fixed number of neighboring memory elements;

~~(c) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;~~

b) steps for concurrently defining an new array within an existing array;

c) steps for concurrently performing a same operation on all array items of said array;

d) steps for concurrently finding ~~none of the~~ in said array no array item satisfying ~~the comparison~~ a value matching requirement;

e) steps for concurrently finding ~~the highest address of the array item which satisfies the comparison requirement~~ in said array the array item which (A) satisfies a value matching requirement, and (B) has the highest index;

f) steps for concurrently finding ~~the lowest address of the array item which satisfies the comparison requirement~~ in said array the array item which (A) satisfies a value matching requirement, and (B) has the lowest index;

g) steps for concurrently enumerating in said array the array items each of which satisfies ~~the comparison~~ a value matching requirement;

h) steps for finding a global ~~boundaries of~~ value bound to said ~~the~~ array by concurrent steps;

i) steps for finding a global ~~limit~~ extreme value of ~~the~~ said array by concurrent steps; and

75 (Currently amended) An apparatus of Claim 73, further comprising:

a) a parallel counter, comprising:

1) a plurality of bit inputs,

2) a count output, and

3) means for concurrently counting ~~the~~ said bit inputs which are positively asserted;

b) means for connecting ~~(1)~~ ~~the~~ each match bit output ~~of each~~ of all ~~the~~ said memory elements to a unique bit input of ~~the~~ said parallel counter; and

~~(2) the count output of the parallel counter to the input/output control unit;~~

c) said finding means further comprising counting means for concurrently counting said enabled memory elements whose match bit outputs are positively asserted.

~~(c) the concurrent means further comprising:~~

~~(1) matching means for specifying the required state for matching concurrently to all the memory elements by the data stored in each enabled memory element and a matching requirement; and~~

~~(2) counting means for concurrently counting the enabled memory elements whose match bit outputs are positively asserted; and~~

~~(d) the instruction means further comprising:~~

~~(1) means for concurrently specifying a matching requirement to each of all the memory elements; and~~

~~(2) means for writing the count of the enabled memory elements which satisfy the matching requirement to the external connection of the apparatus.~~

76 (Currently amended) Steps for using said apparatus of Claim 75 to store and manage an array, further comprising:

~~(a) steps for concurrently specifying a comparison requirement to each of all the memory elements;~~

~~(b) steps for storing an array by the apparatus;~~

a) steps for storing each array item either (1) in each memory element or (2) in each fixed number of neighboring memory elements;

~~(c) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;~~

b) steps for concurrently defining an new array within an existing array;

c) steps for concurrently performing a same operation on all array items of said array;

d) steps for concurrently finding ~~none of the~~ in said array no array item satisfying ~~the comparison~~ a value matching requirement;

e) steps for concurrently finding ~~the highest address of the array item which satisfies the comparison requirement~~ in said array the array item which (A) satisfies a value matching requirement, and (B) has the highest index;

f) steps for concurrently finding ~~the lowest address of the array item which satisfies the comparison requirement~~ in said array the array item which (A) satisfies a value matching requirement, and (B) has the lowest index;

g) steps for concurrently enumerating in said array the array items each of which satisfies ~~the comparison~~ a value matching requirement;

h) steps for concurrently counting in said array the array items each of which satisfies ~~the comparison~~ a value matching requirement;

i) steps for finding a global ~~boundaries of~~ value bound to said ~~the~~ array by concurrent steps;

j) steps for finding a global ~~limit~~ extreme value of ~~the~~ said array by concurrent steps; and

k) steps for constructing a histogram of ~~the~~ said array by concurrent steps.

77-79 (Cancelled)

80 (Currently amended) An apparatus ~~of claim 8, further~~ comprising:

~~a) the concurrent bus carrying concurrently to each of all the memory elements:~~

~~(1) a read selection code; and~~

~~(2) an operation code;~~

~~(b) each of all the memory elements further comprising:~~

~~(1) a shared register, being a register;~~

~~(2) a operation register, being a register; and~~

~~(3) a register multiplexer, being a bus multiplexer, comprising:~~
~~(A) a plurality of inputs;~~
~~(B) an output; and~~
~~(C) a selection input, which selects one of the inputs to be connected to the output; and~~
~~(4) means for connecting:~~
~~(A) the shared register to a unique input of the register multiplexer;~~
~~(B) the operation register to the output of the register multiplexer; and~~
~~(C) the read selection code of the concurrent bus to the selection input of the register multiplexer;~~
~~(c) neighboring means for connecting each of all the memory elements to other memory elements, the neighboring means further comprising:~~
~~(1) up connecting means for connecting from the shared register of each of all the memory elements to a unique input of the register multiplexer of the memory element which has immediately higher element address; and~~
~~(2) down connecting means for connecting from the shared register of each of all the memory elements to a unique input of the register multiplexer of the memory element which has immediately lower element address;~~
a) a plurality of memory elements, each of which comprising:
1) at least one register, comprising:
A) at least one addressable register; and
B) a shared register;
2) an enable bit input;
3) an instruction input, comprising a select bit;
4) execution means for carrying out instructions at said instruction input only when said enable bit input is positively asserted;
5) a unique element address;
6) only when said enable bit input is positively asserted, neighboring means for reading the shared register of the neighboring memory element whose element address is either (A) immediately lower when said select bit is negatively asserted, or (B) immediately higher when said select bit is positively asserted.
~~(d) the concurrent means further comprising:~~
~~(1) instructing means for sending an instruction to each of all the memory elements using the concurrent bus;~~
~~(2) read selecting means for selecting the same one of the inputs to the output of the register multiplexer of each of all the enabled memory elements;~~
~~(3) read means for copying the content of the output of the register multiplexer to the operation register of each of all the enabled memory elements; and~~
~~(4) write means for copying the content of the operation register to the shared register of each of all the enabled memory elements.~~
b) an input/output control unit, comprising:
1) an external bus connection, and
2) communication means for communicating with said external bus;
c) exclusive means for exclusively copying either (1) the content of any said addressable register to said external bus connection, or (2) the content of said external bus connection to any said addressable register;

d) concurrent means for concurrently executing a same instruction in one or a plural of said memory elements, said concurrent means further comprising:
   1) instructing means for sending said instruction concurrently to all said memory elements;
   2) enabling means for concurrently positively asserting said enable bit inputs of all said memory elements whose element addresses are (A) no less than a start element address, (B) no more than an end element address, and (C) an integer increment of a carry number starting from said start element address; and
   3) executing means for concurrently executing said instruction in all enabled memory elements; and
e) instruction means for receiving and carrying out instructions at said external bus connection, further comprising:
   1) command means for translating the content at said external bus connection into said exclusive means and said concurrent means;
   2) result means for presenting the execution result of said command means at said external bus connection.

81 (Currently amended) An apparatus of Claim 80, wherein:
a) each of ~~its~~ said memory elements further comprises:
   1) ~~the neighboring~~ said addressable register being said shared register;
   ~~(2) the register multiplexer having two inputs; and~~
   2) an operation register;
   ~~(3) only two registers within each memory element;~~
   3) said instruction input further comprises a self bit,
   4) self means for copying the content of said operation register to said addressable register when said self bit is positively asserted; and
   5) said neighboring means further comprising means for copying the content of the addressable register of said neighboring memory element to said operation register when said self bit is negatively asserted;
b) a range decoder, comprising:
   1) a start address input;
   2) an end address input;
   3) a plurality of bit outputs, each of which has a unique address; and
   4) means for concurrently positively asserting all ~~the~~ said bit outputs whose addresses are: (A) no less than the value at ~~the~~ said start address input, and (B) no more than the value at ~~the~~ said end address input, while negatively asserting all ~~the~~ other said bit outputs;
c) means for connecting each ~~the~~ said memory element to a unique bit output of ~~the~~ said range decoder wherein the element address of said memory element equals the corresponding bit output address of said range decoder~~, thus each of all the memory elements having a unique element address~~;
d) ~~the~~ said enabling means further comprising means for using said range decoder to enable all said memory elements, wherein said carry number is a constant one ~~positively asserting the enable bit inputs of the memory elements whose element addresses are: (A) no less than a start address, and (B) no more than an end address~~; and

e) ~~the~~ said concurrent means further comprising:
   ~~1) moving means for concurrently moving the content of all the addressable registers within a register address range either up or down by one addressable register.~~
   1) up moving means for concurrently moving the content of each of all addressable registers within an address range to the addressable register whose address is immediately higher; and
   2) down moving means for concurrently moving the content of each of all addressable registers within an address range to the addressable register whose address is immediately lower.

~~f) the input/output control unit further comprising:~~
   ~~1) controlling means for providing the start address input and the end address input to the range decoder.~~

82 (Currently amended) A preferred implementation of apparatus of Claim 81, wherein said ~~its~~ operation registers are made of dynamic memory cells whose storage duration is only long enough for carrying out said moving means.

83 (Currently amended) An apparatus of Claim 81, ~~its moving means~~ further comprising moving means for concurrently moving the content of all the addressable registers within ~~a register~~ an address range to another ~~register~~ address range of the same size.

84 (Currently amended) Content moving means for moving within ~~the~~ said apparatus of Claim 81, a data object which occupies a continuous ~~register~~ address range, ~~the~~ said content moving means further comprising:
a) moving means for moving a data object within ~~the~~ said apparatus to another register address range without overwriting any other ~~useful~~ stored data;
b) inserting means for inserting a data object into ~~the~~ said apparatus without overwriting any other ~~useful~~ stored data;
c) enlarging means for enlarging a data object within ~~the~~ said apparatus without overwriting any other ~~useful~~ stored data;
d) shrinking means for shrinking a data object within the apparatus without leaving unused addressable registers at where ~~the~~ said data object originally resides;
e) removing means for removing a data object from ~~the~~ said apparatus without leaving unused addressable registers at where the data object originally resides; and
f) packing means for keeping the used portion of the addressable registers adjacent to each other so that the data within ~~the~~ said apparatus are closely packed during inserting, enlarging, shrinking, removing, and moving data object within ~~the~~ said apparatus.

85 (Currently amended) Address independent means for identifying the stored data objects within an apparatus which has content moving means as claimed in claim 84, ~~each by a unique number independent of the addresses which are associated with the storing of the data object in the apparatus~~, ~~the~~ said address independent means comprising:

a) means for identifying each data objects ~~in the apparatus~~ by an object ID which is a unique number, independent of the addresses which are associated with the storing of ~~the~~ said data object ~~in the apparatus~~;
b) means for adding a new data object of a specified size and obtaining the corresponding new object ID;
c) means for removing a such identified data object;
d) means for changing the size of a such identified object by specifying a new size of ~~the~~ said data object;
e) means for exclusively accessing any part of a such identified data object by an offset into ~~the~~ said data object;
f) means for refusing access when a such access is beyond the storage range of ~~the~~ a such identified data object; and
g) means for containing a child data object within a parent data object, and (1) adjusting the size of ~~the~~ said parent data object accordingly when operating any of ~~its~~ said child data objects; and (2) adjusting the size and location of ~~the~~ said child data object when operating any of ~~its~~ said parent object.

86-89 (Cancelled)

90 (Currently amended) An apparatus of Claim ~~89~~91, wherein ~~each of all its memory elements further comprising~~:
a) ~~all the registers are addressable~~ every register in each said memory element is addressable; and
b) while performing a task comprising a set of said concurrent means and said exclusive means, steps for concurrently update the addressable registers which are not involved in said on-going task, to prepare said addressable registers for the next task to be performed.

91 (Currently amended) An apparatus of Claim 8, wherein said concurrent means and said exclusive means can be carried out concurrently provided that they do not operate on a same register simultaneously. ~~Task switching steps for alternatively operating on a plurality of arrays stored in the apparatus of claim 90, the task switching steps further comprising:~~
~~a) steps for using one set of data registers to store data for a task in each memory element which are used by the task; and~~
~~b) while operating on the set of data registers in each memory element which are used by the task, steps for updating all other data registers in each memory element which are used by the task and all registers of the memory elements which are not used by the task.~~

92 (Currently amended) An apparatus ~~of claim 80, each memory element further~~ comprising:
a) a plurality of memory elements, each of which comprising:
1) at least one register, comprising:
A) at least one addressable register; and
B) a shared register;

2) an enable bit input;
3) an instruction input, comprising a select bit;
4) execution means for carrying out instructions at said instruction input only when said enable bit input is positively asserted;
5) a unique element address;
6) only when said enable bit input is positively asserted, neighboring means for reading the shared register of the neighboring memory element whose element address is either (A) immediately lower when said select bit is negatively asserted, or (B) immediately higher when said select bit is positively asserted;
7) a match bit output;
8) state means for defining states for ~~the~~ said memory element ~~when it is enabled~~; and
~~(b) conditional means for carrying out operation code on the concurrent bus when the memory element is in a required state.~~
9) matching means for positively asserting said match bit output only when said memory element is in a required state and said enable bit input is positively asserted;

b) an input/output control unit, comprising:
1) an external bus connection, and
2) communication means for communicating with said external bus;

c) exclusive means for exclusively copying either (1) the content of any said addressable register to said external bus connection, or (2) the content of said external bus connection to any said addressable register;

d) concurrent means for concurrently executing a same instruction in one or a plural of memory elements, said concurrent means further comprising:
1) enabling means for concurrently positively asserting said enable bit inputs of all said memory elements whose element addresses are (A) no less than a start element address, (B) no more than an end element address, and (C) an integer increment of a carry number starting from said start element address;
2) instructing means for sending said instruction concurrently to all said memory elements;
3) executing means for concurrently executing said instruction in all enabled memory elements;
4) matching request means for using a required state for matching concurrently at all enabled memory elements; and
5) finding means for concurrently finding said memory elements whose match bit outputs have been positively asserted; and

h) instruction means for receiving and carrying out instructions at said external bus connection, further comprising:
1) command means for translating the content at said external bus connection into said exclusive means and said concurrent means;
2) result means for presenting the execution result of said command means at said external bus connection.

93 (Cancelled)

94 (Currently amended) An apparatus of Claim 92, ~~each memory element further comprising the required state being a predefined state~~ wherein said required state of matching of said memory elements is predefined.

95 (Currently amended) An apparatus of Claim 92, ~~further comprising~~ wherein:

a) ~~the concurrent bus further carrying~~ said instruction means further comprises means for sending a condition ~~specification~~ code to ~~each of all the~~ said memory elements; and

b) ~~the~~ said matching means further ~~comprising~~ comprises ~~(1) specifying~~ means for ~~using the~~ translating said condition ~~specification~~ code ~~of the concurrent bus~~ to ~~specify the~~ said required state of matching~~, and (2)determining means for determining if the state of the memory element matches the required state which has been specified by the condition specification of the concurrent bus~~.

96-98 (Cancelled)

99 (Currently amended) An apparatus of Claim ~~96~~106, further comprising:

a) a priority encoder, comprising:

1) a plurality of bit inputs, each of which ~~corresponds to~~ has a unique address;

2) a no-hit bit output, which is positively asserted only when none of ~~the~~ said bit inputs is positively asserted;

3) a priority high bit input;

4) an address output, ~~when the no-hit bit output being negatively asserted, the address output~~ which containing either (A) the highest address of ~~the~~ said bit inputs which are positively asserted when ~~the~~ said priority high bit input is positively asserted, or (B) the lowest address of ~~the~~ said bit inputs which are positively asserted when ~~the~~ said priority high bit input is negatively asserted;~~ and~~

b) means for connecting ~~(1) the~~ each match bit output ~~of each~~ of all ~~the~~ said memory elements to a unique bit input of ~~the~~ said priority encoder wherein the element address of each said memory element equals the corresponding bit input address of said priority encoder; and~~, thus each of all the memory elements having an address~~;

~~(2) the priority high bit input of the priority encoder from the input/output control unit; and~~

~~(3) the no-hit bit output and the address output of the priority encoder to the input/output control unit;~~

c) said finding means further comprising:

1) means for finding no said enabled memory elements whose match bit outputs are positively asserted; and

2) means for finding either (A) the highest or (B) the lowest element address of said enabled memory elements whose match bit outputs are positively asserted.

~~(c) the concurrent means further comprising:~~

~~(1) matching means for defining the required state for the conditional means concurrently to all the memory element by the data stored in each enabled memory element and a matching requirement;~~

~~(2) null means for signaling none of the enabled memory elements whose match bit output is positively asserted; and~~

~~(3) addressing means for finding either (A) the highest or (B) the lowest address of the enabled memory element whose match bit output is positively asserted; and~~

~~(d) the instruction means further comprising:~~

~~(1) means for concurrently specifying a matching requirement to all the memory elements;~~

~~(2) means for writing a predefined value to the external connection of the apparatus if no enabled memory element satisfying the matching requirement; and~~

~~(3) means for writing to the external connection of the apparatus either (A) the highest or (B) the lowest address of the enabled memory element which satisfies the matching requirement.~~

100 (Currently amended) Steps for using apparatus of Claim 99 to store and manage arrays, further comprising:

a) steps for storing each array item either (1) in each memory element or (2) in each fixed number of neighboring memory elements;

~~(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;~~

b) steps for concurrently defining an array within an existing array;

~~(b) steps for concurrently specifying a matching requirement to each of all the memory elements;~~

c) steps for concurrently performing a same operation on all array items of said array;

d) steps for concurrently finding ~~none of the enabled memory elements~~ in said array no array item satisfying a value matching requirement;

e) steps for concurrently finding ~~the highest address of the enabled memory elements which satisfies the matching requirement~~ in said array the array item which (1) satisfies a value matching requirement, and (2) has the highest index;

f) steps for concurrently finding ~~the highest address of the enabled memory elements which satisfies the matching requirement~~ in said array the array item which (1) satisfies a value matching requirement, and (2) has the lowest index;

g) steps for concurrently enumerating ~~the addresses of the enabled memory elements~~ in said array the array items each of which satisfies a value matching requirement;

h) steps for finding a global value bound to said array by concurrent steps;

i) steps for finding a global extreme value of said array by concurrent steps; and

101 (Currently amended) An apparatus of Claim 99, further comprising:

a) a parallel counter, comprising:
   1) a plurality of bit inputs,
   2) a count output, and
   3) means for concurrently counting ~~the~~ said bit inputs which are positively asserted;

b) means for connecting ~~(1) the~~ each match bit output of ~~each of~~ all ~~the~~ said memory elements to a unique bit input of ~~the~~ said parallel counter, and

~~(2) the count output of the parallel counter to the input/output control unit;~~

c) said finding means further comprising counting means for concurrently counting said enabled memory elements whose match bit outputs are positively asserted.

~~(c) the concurrent means further comprising:~~

~~(1) matching means for specifying the required state for the conditional means concurrently to all the memory element by the data stored in each enabled memory element and a matching requirement; and~~

~~(2) counting means for concurrently counting the enabled memory element whose match bit outputs are positively asserted; and~~

~~(d) the instruction means further comprising:~~

~~(1) means for concurrently specifying a matching requirement to all the memory elements; and~~

~~(2) means for writing the count of the enabled memory elements each of which satisfies the matching requirement to the external connection of the apparatus.~~

102 (Currently amended) Steps for using apparatus of Claim 101 to store and manage arrays, further comprising:

a) steps for storing each array item either (1) in each memory element or (2) in each fixed number of neighboring memory elements;

~~(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;~~

b) steps for concurrently defining an array within an existing array;

~~(b) steps for concurrently specifying a matching requirement to each of all the memory elements;~~

c) steps for concurrently performing a same operation on all array items of said array;

d) steps for concurrently finding ~~none of the enabled memory elements~~ in said array no array item satisfying a value matching requirement;

e) steps for concurrently finding ~~the highest address of the enabled memory elements which satisfies the matching requirement~~ in said array the array item which (1) satisfies a value matching requirement, and (2) has the highest index;

f) steps for concurrently finding ~~the highest address of the enabled memory elements which satisfies the matching requirement~~ in said array the array item which (1) satisfies a value matching requirement, and (2) has the lowest index;

g) steps for concurrently enumerating ~~the addresses of the enabled memory elements~~ in said array the array items each of which satisfies a value matching requirement;

h) steps for concurrently counting ~~the enabled memory elements~~ in said array the array items each of which satisfies a value matching requirement;

i) steps for finding a global value bound to said array by concurrent steps;

j) steps for finding a global extreme value of said array by concurrent steps; and

k) steps for constructing a histogram of said array by concurrent steps.

103 (Currently amended) An apparatus of Claim 92, further comprising:

a) a general decoder, comprising:

1) a start address input;

2) an end address input;

3) a carry number input;

4) a plurality of bit outputs, each of which has a unique address; and

5) means for concurrently positively asserting all ~~the~~ said bit outputs whose addresses are: (A) no less than the value at ~~the~~ said start address input, (B) no more than the value at ~~the~~ said end address input, and (C) an integer increment of

the value at ~~the~~ said carry number input starting from the value at ~~the~~ said start address input, while negatively asserting all ~~the~~ other said bit outputs;

b) means for connecting each of all ~~the~~ said memory elements to ~~the~~ a unique bit output of ~~the~~ said general decoder ~~which has the same address as the memory element~~ wherein the element address of each said memory element equals the corresponding bit output address of said range decoder

c) ~~the~~ said enabling means further comprising means for ~~positively asserting the enable bit inputs of~~ using the general decoder to enable all ~~the~~ said memory elements. ~~whose element addresses are (1) no less than a start element address, (2) no more than an end element address, and (3) an integer increment of a carry number starting from the start element address; and~~

~~d) the input/output control unit further comprising controlling means for providing the start address input, the end address input and the carry number input to the general decoder.~~

104 (Currently amended) An apparatus of claim ~~103~~181, further comprising dividing means for ~~obtaining (A) the quotient and (B) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset~~ dividing a dividend by a divisor to obtain the quotient and the remainder of said division, wherein said dividend equals the value of subtracting an offset from a subtrahend, said ~~the~~ dividing means further comprising:

a) means for inputting ~~the~~ said offset into ~~the~~ said start address input of ~~the~~ said general decoder;

b) means for inputting ~~the~~ said subtrahend to ~~the~~ said end address input of ~~the~~ said general decoder;

c) means for inputting ~~the~~ said divider to ~~the~~ said carry number input of ~~the~~ said general decoder;

d) means for connecting each of all bit outputs of ~~the~~ said general decoder to a unique bit input of ~~the~~ said parallel counter~~, except the bit output at address 0 of the general decoder~~;

e) means for outputting from ~~the~~ said count output of ~~the~~ said parallel counter the value of said quotient plus one;

f) means for connecting each of all bit outputs of ~~the~~ said general decoder to a unique ~~the~~ bit input ~~the~~ said priority encoder wherein each bit input address of said priority encoder equals the bit output address of said general decoder ~~which has the same address, except the bit output at address 0 of the general decoder~~;

g) means for positively asserting ~~the~~ said priority high bit input of ~~the~~ said priority encoder;

~~h) when the said no-hit bit output of the said priority encoder is positively asserted, means for signaling the said divider being 0; and~~

h) ~~when the no-hit bit output of the priority encoder is negatively asserted~~, means for outputting the value of said dividend minus said reminder from ~~the~~ said address output of ~~the~~ said priority encoder.~~; and~~

~~i) the instruction means further comprising means for obtaining (1) the quotient, and (2) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset.~~

105 (Currently amended) An apparatus of Claim 104, further comprising:
a) a plurality of bit storage elements;
b) means for connecting:
   1) each enable bit input of all ~~the~~ said memory elements from a unique bit storage element; and
   2) each of all ~~the~~ said bit storage element from a unique bit output of ~~the~~ said general decoder wherein the element address of each said memory element equals the bit output address of said general decoder;
c) said enabling means further comprising retaining means for retaining the value of ~~the~~ said bit storage elements when obtaining ~~(1) the quotient, and (2) the value of dividend minus reminder, of dividing a dividend by a divider, the dividend being the value of a subtrahend minus an offset~~ the result of said dividing means, so that said concurrent means and said dividing means can be carried out concurrently.

106 (Currently amended) An apparatus of Claim 92, ~~each of all the memory elements further comprising~~ wherein::
~~(a) a value comparator, comprising:~~
   ~~(1) a first input;~~
   ~~(2) a second input;~~
   ~~(3) an equal bit output, which is positively asserted when the value of the first input equals the value of the second input; and~~
   ~~(4) a larger bit output, which is either (A) positively asserted when the value at the first input is larger than the value at the second input, or (B) negatively asserted when the value at the first input is smaller than the value at the second input;~~
~~(b) means for connecting:~~
   ~~(1) the output of the register multiplexer to the first input of the value comparator; and~~
   ~~(2) the operation register to the second input of the value comparator; and~~
~~(c) the state means further comprising means for using (A) the equal bit output of the value comparator and (B) the larger bit output of the value comparator to define the state of the memory element.~~
a) each said memory element further comprises:
   1) only one addressable register;
   2) said instruction input further comprising:
      A) a datum;
      B) a comparison code, specifying the condition of either (i) equal, or (ii) unequal, or (iii) greater than, or (iv) less than, or (v) greater than or equal, or (vi) less than or equal; and
      C) an operation code, comprising a self bit; and a transfer bit;
   3) a value comparator, comparing said datum and said addressable register, and outputting a comparison result;
   4) said shared register further comprising a match bit; and
   5) asserting means for asserting said match bit when said enabled bit input is positively asserted, said asserting means further comprising:

A) when said self bit is positively asserted, means for positively asserting said match bit only when said comparison result meets said comparison code; or

B) when (i) said self bit is negatively asserted, and (ii) said transfer bit is negatively asserted, means for positively asserting said match bit only when (i) said comparison result meets said comparison code, and (ii) the match bit of said neighboring memory element is positively asserted; or

C) when (i) said self bit is negatively asserted, (ii) said transfer bit is positively asserted, means for copying the value of the match bit of said neighboring memory element to said match bit only when said match bit is originally positively asserted; or

D) when (i) said self bit is negatively asserted, (ii) said transfer bit is positively asserted, means for positively asserting said match bit only when (i) said comparison result meets said comparison code, and (ii) said match bit is originally negatively asserted;

6) said matching means further comprising means for positively asserting said match bit output only when said match bit is positively asserted; and

b) said concurrent means further comprising:

1) means for concurrently finding any value match between (A) a value and (B) the content of said addressable register of each enabled memory elements; and

2) means for concurrently finding any value match between (A) a value and (B) the combined content of addressable registers of each enabled neighboring memory elements.

107 (Cancelled)

108 (Currently amended) An apparatus of claim 92, wherein each of ~~its~~ said memory elements further comprising:

a) at least one status bit;

b) status means for either positively or negatively asserting any of ~~the~~ said status bits, and

c) ~~the~~ said state means further comprising means for using the values of ~~the~~ said status bits to define ~~the~~ said state of ~~the~~ said memory element.

109-111 (Cancelled)

112 (Currently amended) An apparatus of Claim ~~106~~92, wherein:

~~(a) the concurrent bus further carrying a condition code to each of all the memory elements;~~

a) each said memory element further comprises:

~~(1) a control unit, comprising:~~

~~(A) an operation code input;~~

~~(B) executing means for executing an operation code at the operation code input;~~

~~(C) an condition code input;~~

~~(D) determining means for determining if the state of the memory element matches the required state which has been specified by an condition code at the condition code input; and~~

~~(E) conditional means for carrying out the executing means when the memory element is in the required state; and~~

~~(2) means for connecting:~~

~~(A) the operation code of the concurrent bus to the control unit;~~

~~(B) the condition code of the concurrent bus to the control unit; and~~

~~(C) the larger bit output and the equal bit output of the value comparator to the control unit; and~~

1) an operation register;
2) an status register comprising a status bit;
3) at lease one data register;
4) said instruction input further comprising:
   A) a datum;
   B) an operand code, encoding for either (i) said datum, or (ii) said shared register, or (iii) the shared register of said neighboring memory element, or (iv) any of said data registers;
   C) an operation code;
   D) a comparison code, encoding for either (i) equal, or (ii) unequal, or (iii) greater than, or (iv) less than, or (v) greater than or equal, or (vi) less than or equal, or (vii) any; and
   E) a status code bit; and
   F) a logic code;
5) operand selecting means for selecting an operand according to said operand code;
6) said execution means further comprising operation means for carrying out the operation specified by said operation code, said operation means further comprising:
   A) means for positively asserting said match bit output;
   B) means for negatively asserting said match bit output;
   C) means for positively asserting said status bit;
   D) means for negatively asserting said status bit;
   E) means for copying the content of said operand to said operation register;
   F) means for copying the content of said operation register to said operand when said operand is either (i) said shared register, or (ii) any of said data registers;
7) a value comparator comparing said operand and said operation register, and outputting a comparison result;
8) a logic control unit, comprising:
   A) means for positively asserting a comparison logic bit only when said comparison result meets said comparison code;
   B) means for positively asserting a status logic bit only when said status bit and said status code bit are identically asserted; and
   C) condition means for positively asserting a bit output only when the logic combination of (i) said comparison logic bit and (ii) said status logic bit meets said logic code;
9) said enabling means further comprising means for enabling said operation means only when said bit output of said logic control unit is positively asserted; and

b) ~~its~~ said concurrent means further ~~comprising~~ comprises:

~~(1) specifying means for using the condition code of the concurrent bus to specify the required state for the conditional means, and~~

~~(2) determining means for determining if the state of each of all the enabled memory elements matches the required state which has been specified by the condition code of the concurrent bus.~~

1) means for concurrently performing any conditional matching operations within each said enabled memory element; and

2) means for concurrently performing any conditional content moving operations either (A) within each said enabled memory element, or (B) between each said enabled memory element and corresponding said neighboring memory element.

113-114 (Cancelled)

115 (Currently amended) An apparatus of Claim ~~114~~112, wherein said logic control unit of each of ~~its~~ said memory element further comprising:

a) means for positively asserting an operand AND logic bit only when all bits of said operand are positively asserted;

b) means for positively asserting an operand OR logic bit only when any bit of said operand is positively asserted; and

c) means for positively asserting an operation AND logic bit only when all bits of said operation register is positively asserted; and

d) means for positively asserting an operation OR logic bit only when any bit of said operation register is positively asserted; and

e) said condition means further comprising means for positively asserting said bit output only when the logic combination of (1) said comparison logic bit, (2) said status logic bit, (3) either said operand AND bit or said operand OR bit, and (4) either said operation AND bit or said operation OR bit meets said logic code.

~~(a) a first and a second OR gates, each comprising:~~

~~(1) a plurality of bit inputs; and~~

~~(2) a bit output, which is positively asserted when any of the bit inputs is positively asserted;~~

~~(b) a first and a second AND gates, each comprising:~~

~~(1) a plurality of bit inputs; and~~

~~(2) a bit output, which is positively asserted when all of the bit inputs are positively asserted;~~

~~(c) means for connecting:~~

~~(1) each bit of the output of the register multiplexer to a unique bit input of the first OR gate;~~

~~(2) the bit output of the first OR gate to the control unit;~~

~~(3) each bit of the output of the register multiplexer to a unique bit input of the first AND gate;~~

~~(4) the bit output of the first AND gate to the control unit;~~

~~(5) each bit of the output of the operation register to a unique bit input of the second OR gate;~~

~~(6) the bit output of the second OR gate to the control unit;~~

~~(7) each bit of the output of the operation register to a unique bit input of the second AND gate; and~~

~~(8) the bit output of the second AND gate to the control unit;~~

~~(d) the "condition" code for the instruction means comprising any one of the following set:~~

~~(1) the value relation between the operation register and the output of the register multiplexer, comprising any one of: (A) smaller, (B) smaller or equal, (C) equal, (D) not equal, (E) larger or equal, and (F) larger;~~

~~(2) the value of any of the status bits, comprising any one of: (A) positively asserted, and (B) negatively asserted;~~

~~(3) either (A) the AND or (B) the OR combination of all the bit of the output from the register multiplexer;~~

~~(4) either (A) the AND or (B) the OR combination of all the bit of the output from the operation register;~~

~~(5) the AND combination of (1) and (2);~~

~~(6) the OR combination of (1) and (2);~~

~~(7) the AND combination of (1) and (3);~~

~~(8) the OR combination of (1) and (3);~~

~~(9) the AND combination of (1) and (4);~~

~~(10) the OR combination of (1) and (4);~~

~~(11) the AND combination of (2) and (3);~~

~~(12) the OR combination of (2) and (3);~~

~~(13) the AND combination of (2) and (4);~~

~~(14) the OR combination of (2) and (4);~~

~~(15) the AND combination of (3) and (4); and~~

~~(16) the OR combination of (3) and (4);~~

116 (Currently amended) An apparatus of Claim ~~113~~112, further comprising:

~~(a) a parallel counter, comprising:~~

~~(1) a plurality of bit inputs,~~

~~(2) a count output,~~

~~(3) means for concurrently counting the bit inputs which are positively asserted;~~

a) a priority encoder, comprising:

1) a plurality of bit inputs, each of which ~~corresponds to~~ has a unique address;

2) a no-hit bit output, which is positively asserted only when none of ~~the~~ said bit inputs is positively asserted;

3) a priority high bit input;

4) an address output, ~~when the no-hit bit output being negatively asserted, the address output~~ which containing either (A) the highest address of ~~the~~ said bit inputs which are positively asserted when ~~the~~ said priority high bit input is positively asserted, or (B) the lowest address of ~~the~~ said bit inputs which are positively asserted when ~~the~~ said priority high bit input is negatively asserted; ~~and~~

b) means for connecting:

~~(1) the match bit output of each of all the memory elements to a unique bit input of the parallel counter;~~

~~(2) the count output of the parallel counter to the input/output control unit;~~

~~(3) the~~ each match bit output of ~~each of~~ all ~~the~~ said memory elements to a unique bit input of ~~the~~ said priority encoder wherein the element address of each said memory element equals the corresponding bit input address of said priority encoder; and;~~, thus each of all the memory elements having a unique address;~~

~~(4) the priority high bit input of the priority encoder from the input/output control unit; and~~

~~(5) the no-hit bit output and the address output of the priority encoder to the input/output control unit;~~

c) said finding means further comprising:

1) means for finding no said enabled memory elements whose match bit outputs are positively asserted; and

2) means for finding the highest element address of said enabled memory elements whose match bit outputs are positively asserted.

~~(d) the concurrent means further comprising:~~

~~(1) matching means for defining the required state for the conditional means concurrently to all the memory element by the data stored in each enabled memory element and a matching requirement;~~

~~(2) counting means for concurrently counting the enabled memory elements whose match bit outputs are positively asserted;~~

~~(3) null means for signaling none of the enabled memory elements whose match bit output is positively asserted; and~~

~~(4) addressing means for finding either (A) the highest or (B) the lowest element address among the enabled memory elements whose match bit outputs are positively asserted; and~~

~~(e) the instruction means further comprising:~~

~~(1) means for concurrently specifying a matching requirement to each of all the memory elements;~~

~~(2) means for writing to the external connection of the apparatus the count of the enabled memory elements each of which satisfies the matching requirement;~~

~~(3) means for writing a predefined value to the external connection of the apparatus if no enabled memory element satisfying the matching requirement; and~~

~~(4) means for writing to the external connection of the apparatus either (A) the highest or (B) the lowest address among those of the enabled memory elements each of which satisfies the matching requirement.~~

117 (Currently amended) Steps for using apparatus of Claim 187 to store and manage arrays, further comprising:

a) steps for storing array either (1) with each array in each memory element or (2) with each array in each neighboring memory elements or (3) with each memory elements contains a fixed number of array items;

~~(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;~~

b) steps for concurrently defining a new array in an existing array;

~~(b) steps for concurrently specifying a requirement for the conditional means to each of all the memory elements;~~

~~(c) steps for storing an array by the apparatus;~~

c) steps for concurrently performing a same operation on all array items of said array;
d) steps for concurrently finding ~~none of the~~ in said array no array item satisfying ~~the~~ a matching requirement;
e) steps for concurrently finding ~~the highest address of the array item which satisfies the matching requirement~~ in said array the array item which (1) satisfies a matching requirement, and (2) has the highest index;
f) steps for concurrently finding ~~the lowest address of the array item which satisfies the matching requirement~~ in said array the array item which (1) satisfies a matching requirement, and (2) has the lowest index;
g) steps for concurrently enumerating in said array the array items each of which satisfies ~~the~~ a matching requirement;
h) steps for concurrently counting in said array the array items each of which satisfies ~~the~~ a matching requirement;
i) steps for concurrently finding local extreme values of ~~the~~ said array;
j) steps for finding a global ~~limit of~~ value bound to said array by concurrent steps;
k) steps for finding a global extreme value of ~~the~~ said array by concurrent steps;
l) steps for constructing a histogram of ~~the~~ said array by concurrent steps;
m) steps for concurrently inserting a new array item anywhere in ~~the~~ said array while keeping all data closely packed;
n) steps for concurrently deleting an existing array item anywhere in ~~the~~ said array while keeping all data closely packed;
o) steps for concurrently exchanging two existing neighboring array items anywhere in ~~the~~ said array while keeping all data closely packed;
p) steps for concurrently sorting ~~the~~ said array by concurrent steps, and
q) steps for concurrently inserting a new array item properly into a sorted said array.

118-120 (Cancelled)

121 (Currently amended) An apparatus of Claim ~~116~~112, wherein each said memory element further ~~comprising~~ comprises:
~~(a) each of all its memory elements further comprising means for incrementing the operation register;~~
~~(b) the concurrent means father comprising incrementing means for incrementing the operation register of each of all the enabled memory elements.~~
a) an increment register; and
b) said operation means further comprising:
1) means for incrementing said increment register, and
2) means for resetting said increment register.

122 (Currently amended) Steps for using apparatus of Claim 121, further comprising:
~~(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for matching;~~
~~(b) steps for concurrently specifying a requirement for the conditional means to each of all the memory elements;~~
~~(c) steps for storing an array by the apparatus;~~
~~(d) steps for concurrently finding none of the array item satisfying the requirement;~~

~~(e) steps for concurrently finding the highest address among the array item each of which satisfies the requirement;~~
~~(f) steps for concurrently finding the lowest address of the array item which satisfies the requirement;~~
~~(g) steps for concurrently enumerating addresses of the array items each of which satisfies the requirement;~~
~~(h) steps for concurrently counting the array items each of which satisfies the requirement;~~
~~(i) steps for concurrently constructing a histogram of the array;~~
~~(j) steps for concurrently finding the degree of matching each of all the array item against the requirement;~~
~~(k) steps for concurrently finding the local extreme values of the array;~~
~~(l) steps for concurrently finding the local extreme values of the array with a difference threshold;~~
~~(m) steps for concurrently finding a global limit of the array;~~
~~(n) steps for concurrently finding a global extreme value of the array;~~
~~(o) steps for concurrently sorting the array;~~
~~(p) steps for concurrently inserting a new array item anywhere in the array;~~
~~(q) steps for concurrently deleting a existing array item anywhere in the array; and~~
~~(r) steps for concurrently exchanging two existing array items anywhere in the array.~~
a) steps for separating a matching requirement into steps of matching requirements;
b) steps for concurrently incrementing said increment register of each said enabled memory element which meets a step of said match requirement; and
c) steps for using the value of said increment register of each said enabled memory element as a degree indicator for meeting said matching requirement.

123 (Currently amended) An apparatus of Claim ~~113~~112, ~~each of all its memory elements further comprising~~ wherein:
a) each said memory element further comprises:
1) said status register further comprising a carry bit;
2) an adder, comprising:
A) a first input;
B) a second input;
C) a carry bit input; and
D) a sum output and a carry bit output, which holds the sum ~~value~~ of adding ~~the values of the~~ said carry bit input, ~~the~~ said first input, and ~~the~~ said second input; and;
~~E) a carry bit output, which holds the sum value of adding the values of the carry bit input, the first input, and the second input; and~~;
~~(c) a operation multiplexer, being a bus multiplexer, comprising:~~
~~(1) a plurality of inputs;~~
~~(2) an output; and~~
~~(3) a selection input, which selects one of the inputs to the output;~~
3) means for connecting:
A) said first input of said adder from said operation register;
B) said second input of said adder from said operand;
C) said sum output of said adder to said operation register;

D) said carry bit input of said adder from said carry bit; and
E) said carry bit output of said adder to said carry bit;
~~(1) the carry bit to the carry bit input of the adder;~~
~~(2) the carry bit from the carry bit output of the adder;~~
~~(3) the output of the register multiplexer to the first input of the adder;~~
~~(4) the operation register to the second input of the adder;~~
~~(5) the sum output of the adder to a unique input of the operation multiplexer;~~
~~(6) the output of the register multiplexer to a unique input of the operation multiplexer;~~
~~(7) the output of the operation multiplexer to the operation register; and~~
~~(8) the selection input of the operation multiplexer from the operation code of the concurrent bus; and~~

4) said operation means further comprising :
A) means for positively asserting said carry bit of the status register;
B) means for negatively asserting said carry bit of the status register; and
C) means for adding said operand to said operation register; and
5) said instruction input further comprising a carry code bit;
6) said logic control unit further comprising:
A) means for positively asserting a carry logic bit only when said carry bit and said carry code bit are identically asserted; and
B) said condition means further comprising means for positively asserting said bit output only when the logic combination of (A) said comparison logic bit and (B) said status logic bit and (C) said carry logic bit meets said logic code;

b) said concurrent means further comprising:
1) means for concurrently performing any conditional adding operations within each said enabled memory element.

124 (Cancelled)

125 An apparatus of Claim ~~1~~24123, ~~further comprising~~ wherein:
a) each said memory element further comprising:
1) ~~the~~ said adder ~~parallel in each of all its memory elements~~ further comprising:
A) an AND output; which holds ~~means for outputting to the AND output, the result of~~ bitwise AND combination of ~~combining the values of the~~ said first input and ~~the~~ said second input;
B) an OR output; which holds ~~means for outputting to the OR output, the result of~~ bitwise OR combination of ~~combining the values of the~~ said first input and ~~the~~ said second input;
C) a XOR output; which holds ~~means for outputting to the XOR output, the result of~~ bitwise XOR combination of ~~combining the values of the~~ said first input and ~~the~~ said second input; and
D) a NOT output; which holds bitwise NOT of said second input; and
~~(b) means for connecting:~~
~~(1) the AND output of the parallel adder to a unique input of the operation multiplexer;~~

~~(2) the OR output of the parallel adder to a unique input of the operation multiplexer; and~~

~~(3) the XOR output of the parallel adder to a unique input of the operation multiplexer;~~

2) operation selecting means for copying an output of said adder to said operation register according to said operation code;

3) said operation means further comprising:

A) means for outputting bitwise NOT of said operand;

B) means for subtracting said operand from said operation register;

C) means for masking said operation register by bitwise AND with said operand;

D) means for masking said operation register by bitwise AND with the bitwise NOT of said operand;

E) means for masking said operation register by bitwise OR with said operand;

F) means for masking said operation register by bitwise OR with the bitwise NOT of said operand;

G) means for masking said operation register by bitwise XOR with said operand;

H) means for masking said operation register by bitwise XOR with the bitwise NOT of said operand;

b) ~~its~~ said concurrent means further comprising:

~~(1) AND means for bitwise logically AND combining the values of (A) the operation register, and (B) the register specified by the read selection code, and means for copying the result to the operation register;~~

~~(2) OR means for bitwise logically OR combining the values of (A) the operation register, and (B) the register specified by the read selection code, and means for copying the result to the operation register; and~~

~~(3) XOR means for bitwise logically XOR combining the values of (A) the operation register, and (B) the register specified by the read selection code, and means for copying the result to the operation register.~~

1) means for concurrently performing conditional bitwise logic operations within each enabled memory element;

2) means for concurrently performing conditional addition/subtraction arithmetic operations within each enabled memory element; and

3) means for concurrently performing conditional general arithmetic operations within each enabled memory element.

126-128 (Cancelled)

129 (Currently amended) Steps for using apparatus of Claim ~~123~~193 to store and manage arrays, further comprising:

~~(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for operating upon;~~

~~(b) steps for concurrently specifying a requirement for the conditional means to each of all the memory elements;~~

~~(c) steps for storing an array by the apparatus;~~

a) steps for storing array either (1) with each array in each memory element or (2) with each array item in each fixed number of neighboring memory elements or (3) with each memory elements contains a fixed number of array items;
b) steps for concurrently defining a new array within an existing array;
c) steps for concurrently performing a same operation on all array items of said array;
d) steps for concurrently finding ~~none of the~~ in said array no array item satisfying ~~the~~ a matching requirement;
e) steps for concurrently finding ~~the highest address of the array item which satisfies the matching requirement~~ in said array the array item which (1) satisfies a matching requirement, and (2) has the highest index;
f) steps for concurrently finding ~~the lowest address of the array item which satisfies the matching requirement~~ in said array the array item which (1) satisfies a matching requirement, and (2) has the lowest index;
g) steps for concurrently enumerating in said array the array items each of which satisfies ~~the~~ a matching requirement;
h) steps for concurrently counting in said array the array items each of which satisfies ~~the~~ a matching requirement;
i) steps for concurrently finding local extreme values of ~~the~~ said array;
~~(l) steps for concurrently finding the local extreme values of the array with a difference threshold;~~
j) steps for finding a global ~~limit of~~ value bound to said array by concurrent steps;
k) steps for finding a global extreme value of ~~the~~ said array by concurrent steps;
l) steps for constructing a histogram of ~~the~~ said array by concurrent steps;
m) steps for concurrently inserting a new array item anywhere in ~~the~~ said array while keeping all data closely packed;
n) steps for concurrently deleting an existing array item anywhere in ~~the~~ said array while keeping all data closely packed;
o) steps for concurrently exchanging two existing neighboring array items anywhere in ~~the~~ said array while keeping all data closely packed;
p) steps for concurrently sorting ~~the~~ said array by concurrent steps, and
q) steps for concurrently inserting a new array item properly into a sorted said array.
r) steps for numerical characterization of said array by concurrent steps;
s) steps for concurrently finding the degree of matching of each ~~of all the~~ array item of said array for a matching requirement;
t) steps for concurrently carrying out a local logic/arithmetic operation involve neighboring array items by concurrent steps;
u) steps for concurrently matching a template against neighboring array items of ~~the~~ said array by concurrent steps;
v) steps for concurrently carrying out certain global logic/arithmetic operations that treat each array item of said array equally by concurrent steps.

130 (Currently amended) An apparatus of Claim ~~123~~194, further comprising:
a) a X general decoder and a Y general decoder, each general decoder comprising:
   1) a start address input;
   2) an end address input;
   3) a carry number input;

4) a plurality of bit outputs, each of which has a unique address; and
5) means for concurrently positively asserting all the bit outputs whose addresses are: (1) no less than the value at the start address input, (2) no more than the value at the end address input, and (3) an integer increment of the value at the carry number input starting from the value at the start address input, while negatively asserting all the other bit outputs; and

b) means for connecting:
1) each of all the memory elements to ~~a unique~~ the bit output of the X general decoder which has the same X address~~, thus each of all the memory elements having a unique X address~~;
2) each of all the memory elements to ~~a unique~~ the bit output of the Y general decoder which has the same Y address~~, thus each of all the memory elements having a unique Y address~~; and
3) the enable bit of each of all memory elements by logic AND combination of:
A) a bit output from the X general decoder with the address of the bit output being identical to the X address of the element address; and
B) a bit output from the Y general decoder with the address of the bit output being identical to the Y address of the element address

c) the enabling means of its concurrent means further comprising XY means for ~~positively asserting the enable bit inputs of~~ using the X general decoder and the Y general decoder to enable all the memory elements:
1) whose X addresses are: (A) no less than the X start address, (B) no more than the X end address, and (C) an integer increment of the X carry number starting from the X start address; and
2) whose Y addresses are: (A) no less than the Y start address, (B) no more than the Y end address, and (C) an integer increment of the Y carry number starting from the Y start address.

~~(e) the neighboring means further comprising:~~
~~(1) left connecting means for connecting from the shared register of each of all the memory elements to a unique inputs of the register multiplexer of the memory element which has immediately lower X address but same Y address;~~
~~(2) right connecting means for connecting from the shared register of each of all the memory elements to a unique input of the register multiplexer of the memory element which has immediately higher X address but same Y address;~~
~~(3) bottom connecting means for connecting from the shared register of each of all the memory elements to a unique inputs of the register multiplexer of the memory element which has immediately lower Y address but same X address; and~~
~~(4) top connecting means for connecting from the shared register of each of all the memory elements to a unique input of the register multiplexer of the memory element which has immediately higher Y address but same X address.~~

131 (Currently amended) Steps for using apparatus of Claim 204 to store and manage arrays, further comprising:
~~(a) steps for concurrently defining or concurrently changing the selection of the enabled memory elements for operating upon;~~

~~(b) steps for concurrently specifying a requirement for the conditional means to each of all the memory elements;~~
~~(c) steps for storing an array by the apparatus;~~
a) steps for storing array either (1) with each array in each memory element or (2) with each array item in each fixed number of neighboring memory elements or (3) with each memory elements contains a fixed number of array items;
b) steps for concurrently defining a new array of the same dimension within an existing array;
c) steps for concurrently defining a row array within an existing two dimensional array;
d) steps for concurrently defining a column array within an existing two dimensional array;
e) steps for concurrently finding ~~none of the~~ in said array no array item satisfying ~~the~~ a matching requirement;
~~(e) steps for concurrently finding the highest address among the array item each of which satisfies the requirement;~~
~~(f) steps for concurrently finding the lowest address of the array item which satisfies the requirement;~~
f) steps for concurrently enumerating in said array the array items each of which satisfies ~~the~~ a matching requirement;
g) steps for concurrently counting in said array the array items each of which satisfies ~~the~~ a matching requirement;
h) steps for concurrently finding local extreme values of ~~the~~ said array;
~~(l) steps for concurrently finding the local extreme values of the array with a difference threshold;~~
i) steps for finding a global ~~limit of~~ value bound to said array by concurrent steps;
j) steps for finding a global extreme value of ~~the~~ said array by concurrent steps;
k) steps for constructing a histogram of ~~the~~ said array by concurrent steps;
~~(o) steps for concurrently sorting the array;~~
~~(p) steps for concurrently inserting a new array item anywhere in the array;~~
~~(q) steps for concurrently deleting a existing array item anywhere in the array; and~~
~~(r) steps for concurrently exchanging two existing array items anywhere in the array.~~
l) steps for finding statistical characterization of said array by concurrent steps;
m) steps for finding the degree of matching for a matching requirement by concurrent steps;
n) steps for concurrently carrying out a local logic and arithmetic operation involve neighboring array items;
o) steps for concurrently matching a template against neighboring array items of ~~the~~ said array; and
p) steps for concurrently carrying out certain global logic and arithmetic operations that treat each array item equally.
~~(t) steps for concurrently finding the sum of neighboring array items;~~
~~(v) steps for concurrently detecting all lines at the atan(Mx / My) direction on an image, in which Mx and My are both integer; and~~
~~(w) steps for concurrently detecting all lines at all directions on an image.~~

132-169 (Cancelled)

170 (New) An apparatus of Claim 11, wherein said instruction kernel is programmable.

171 (New) An apparatus of Claim 8, wherein the value of said carry number of said enabling means is a constant one, so that all memory elements within an address range are enabled.

172 (New) An apparatus of Claim 27, further comprising:

a) a range decoder, comprising:
   1) a start address input;
   2) an end address input;
   3) a plurality of bit outputs, each of which has a unique address; and
   4) means for concurrently positively asserting all said bit outputs whose addresses are: (A) no less than the value at said start address input, and (B) no more than the value at said end address input, while negatively asserting all other said bit outputs;
b) means for connecting each said memory element to a unique bit output of said range decoder wherein the element address of each said memory element equals the corresponding bit output address of said range decoder; and
c) said enabling means further comprising means for using said range decoder to enable all said memory elements, wherein said carry number is a constant one.

173 (New) An apparatus of Claim 27, further comprising:

a) a general decoder, comprising:
   1) a start address input;
   2) an end address input;
   3) a carry number input;
   4) a plurality of bit outputs, each of which has a unique address; and
   5) means for concurrently positively asserting all said bit outputs whose addresses are: (A) no less than the value at said start address input, (B) no more than the value at said end address input, and (C) an integer increment of the value at said carry number input starting from the value at said start address input, while negatively asserting all other said bit outputs; and
b) means for connecting each said memory element to said bit output of said general decoder wherein the element address of each said memory element equals the bit output address of said general decoder;
c) said enabling means further comprising means for using said general decoder to enable all said memory elements.

174 (New) An apparatus of Claim 27, further comprising:

a) a priority high encoder, comprising:
   1) a plurality of bit inputs, each of which has a unique address;
   2) a no-hit bit output, which is positively asserted only when none of said bit inputs is positively asserted; and
   3) an address output, which contains the highest address of said bit inputs which are positively asserted;

b) means for connecting each match bit output of all said memory elements to a unique bit input of said priority high encoder wherein the element address of each said memory element equals the corresponding bit input address of said priority high encoder; and;
c) said finding means further comprising:
   1) means for finding no said enabled memory elements whose match bit outputs are positively asserted; and
   2) means for finding the highest element address of said enabled memory elements whose match bit outputs are positively asserted.

175 (New) An apparatus of Claim 27, further comprising:
a) a priority low encoder, comprising:
   1) a plurality of bit inputs, each of which has a unique address;
   2) a no-hit bit output, which is positively asserted only when none of said bit inputs is positively asserted; and
   3) an address output, which contains the lowest address of said bit inputs which are positively asserted;
b) means for connecting each match bit output of all said memory elements to a unique bit input of said priority encoder wherein the element address of each said memory element equals the corresponding bit input address of said priority encoder; and;
c) said finding means further comprising:
   1) means for finding no said enabled memory elements whose match bit outputs are positively asserted; and
   2) means for finding the lowest element address of said enabled memory elements whose match bit outputs are positively asserted.

176 (New) Steps for using apparatus of Claim 81, further comprising:
   1) allocating steps for concurrently allocating a new memory allocation while keeping all memory allocations closely packed using said up moving means;
   2) de-allocating steps for de-allocating an existing memory allocation while keeping all memory allocations closely packed using said down moving means; and
   3) changing steps for changing an existing memory allocation while keeping all memory allocations closely packed using either said up moving means or said down moving means;

177 (New) Steps for using apparatus of Claim 81, further comprising:
   1) allocating steps for concurrently allocating a new memory allocation while keeping all memory allocations closely packed using said down moving means;
   2) de-allocating steps for de-allocating an existing memory allocation while keeping all memory allocations closely packed using said up moving means; and
   3) changing steps for changing an existing memory allocation while keeping all memory allocations closely packed using either said up moving means or said down moving means;

178 (New) A preferred implementation of apparatus of Claim 81, wherein:

a) both said operation registers and said addressable registers are made of dynamic memory cells; and
b) said concurrent means further comprises refreshing means for concurrently refreshing the contents of each addressable registers within an address range by a consecutive allocation and de-allocation of one addressable register which is at the boundary of said address range.

179 (New) Random access steps for using apparatus of Claim 178 at where a static random access memory is traditionally used, said random access means further comprising:
a) steps for using said exclusive means to access an addressable register externally; and
b) steps for using said refreshing means to refresh all addressable registers in-use when none of them is accessed externally.

180 (New) An apparatus of Claim 81, wherein:
a) each of said memory elements further comprising:
   1) said addressable register further comprising an additional even-or-odd bit;
   2) said operation register further comprising an additional even-or-odd bit;
   3) said self means further comprising means for copying said even-or-odd bit of said addressable register to said even-or-odd bit of said operation register; and
   4) said neighboring means further comprising means for copying the even-or-odd bit of the operation register of said neighboring memory element to said even-or-odd bit of said addressable register; and
b) said exclusive means further comprising:
   1) even-or-odd means for calculating said even-or-odd value of any addressable register;
   2) when copying said external bus connection to any addressable register, means for assigning said even-or-odd value of said addressable register to said even-or-odd bit of said addressable register; and
   3) when copying the content of any addressable register to said external bus connection, means for
      A) detecting the disagreement of the even-or-odd bits between said addressable register and said corresponding operation register,
      B) when the two even-or-odd bits agrees, copying the content of said addressable register to said external bus connection; and
      C) when the two even-or-odd bits disagrees, calculating the even-or-odd value of said addressable register, and either (i) copying said addressable register to said external bus connection if said even-or-odd bit of said addressable register is asserted correctly; or (ii) copying corresponding operation register of said addressable register to said external bus connection if said even-or-odd bit of said addressable register is not asserted correctly.

181 (New) An apparatus of Claim 103, further comprising:
a) a priority encoder, comprising:
   1) a plurality of bit inputs, each of which has a unique address;

2) a no-hit bit output, which is positively asserted only when none of said bit inputs is positively asserted;
3) a priority high bit input; and
4) an address output, which contains either (A) the highest address of said bit inputs which are positively asserted when said priority high bit input is positively asserted, or (B) the lowest address of said bit inputs which are positively asserted when said priority high bit input is negatively asserted; and

b) means for connecting each match bit output of all said memory elements to a unique bit input of said priority encoder wherein the element address of each said memory element equals the corresponding bit input address of said priority encoder; and
c) a parallel counter, comprising:
1) a plurality of bit inputs,
2) a count output, and
3) means for concurrently counting said bit inputs which are positively asserted;
d) means for connecting each match bit output of all said memory elements to a unique bit input of said parallel counter; and
e) said finding means further comprising:
1) means for finding no said enabled memory elements whose match bit outputs are positively asserted;
2) means for finding either (A) the highest or (B) the lowest element address of said enabled memory elements whose match bit outputs are positively asserted: and
3) means for concurrently counting said enabled memory elements whose match bit outputs are positively asserted

182 (New) An apparatus of Claim 106, wherein:
a) each said memory element further comprising:
1) said instruction input further comprising a mask;
2) means for masking the content of said addressable register with said mask; and
3) means for comparing said masked content of said addressable register with said datum in said value comparator;
b) said concurrent means further comprising:
1) means for concurrently finding any value match between (A) a value and (B) masked content of addressable register of each enabled memory element; and
2) means for concurrently finding any value match between (A) a value and (B) combined masked content of addressable registers of each enabled neighboring memory elements.

183 (New) An apparatus of Claim 112, wherein:
a) each said memory element further comprises:
1) said instruction input further comprising:
A) an operation bit section code; and
B) an operand bit section code;
2) said operand selecting means further comprising means for selecting the bit section of said operand according to said operand bit section code; and
3) operation selecting means for selecting the bit section of said operation register according to said operation bit section code for said operation means;

b) said concurrent means further comprises:
   1) means for concurrently performing any conditional matching operations on sub-register level within each said enabled memory element; and
   2) means for concurrently performing any conditional content moving operations on sub-register level within each said enabled memory element

184 (New) An apparatus of Claim 112, wherein each said memory element further comprises:
a) said status register comprising a plural of status bit;
b) said instruction input further comprising a plural of status code bits, with each status code bit corresponding to a unique said status bit;
c) said logic control unit further comprising
   1) a plural status logic bit, with each status logic bit corresponding to a unique said status bit;
   2) means for positively asserting a status logic bit only when the corresponding status bit and the corresponding status code bit are identically asserted; and
   3) means for positively asserting said bit output only when the logic combination of said comparison logic bit and said status logic bits meets said logic code.

185 (New) An apparatus of Claim 112, wherein said logic control unit of each said memory element further comprising:
a) means for positively an operation AND logic bit only when all bits of said operation register is positively asserted; and
b) means for positively an operation OR logic bit only when any bit of said operation register is positively asserted; and
c) said condition means further comprising means for positively asserting said bit output only when the logic combination of (1) said comparison logic bit, (2) said status logic bit, (3) either said operation AND bit or said operation OR bit meets said logic code.

186 (New) Steps for using apparatus of Claim 116 to store and manage arrays, further comprising:
a) steps for storing array either (1) with each array in each memory element or (2) with each array in each neighboring memory elements or (3) with each memory elements contains a fixed number of array items;
b) steps for concurrently defining a new array in an existing array;
c) steps for concurrently performing a same operation on all array items of said array;
d) steps for concurrently finding in said array no array item satisfying a matching requirement;
e) steps for concurrently finding in said array the array item which (1) satisfies a matching requirement, and (2) has the highest index;
f) steps for concurrently finding in said array the array item which (1) satisfies a matching requirement, and (2) has the lowest index;
g) steps for concurrently enumerating in said array the array items each of which satisfies a matching requirement;
h) steps for concurrently finding local extreme values of said array;

i) steps for finding a global value bound to said array by concurrent steps;
j) steps for finding a global extreme value of said array by concurrent steps;
k) steps for concurrently inserting a new array item anywhere in said array while keeping all data closely packed;
l) steps for concurrently deleting an existing array item anywhere in the said array while keeping all data closely packed;
m) steps for concurrently exchanging two existing neighboring array items anywhere in said array while keeping all data closely packed;
n) steps for concurrently sorting said array by concurrent steps, and
o) steps for concurrently inserting a new array item properly into a sorted said array.

187 (New) An apparatus of Claim 116, further comprising:
a) a parallel counter, comprising:
   1) a plurality of bit inputs,
   2) a count output, and
   3) means for concurrently counting said bit inputs which are positively asserted;
b) means for connecting each match bit output of all said memory elements to a unique bit input of said parallel counter; and
c) said finding means further comprising counting means for concurrently counting said enabled memory elements whose match bit outputs are positively asserted.

188 (New) An apparatus of Claim 123, wherein:
a) each said memory element further comprises:
   1) said instruction input further comprising:
      A) an operation bit section code; and
      B) an operand bit section code;
   2) said operand selecting means further comprising means for selecting the bit section of said operand according to said operand bit section code; and
   3) operation selecting means for selecting the bit section of said operation register according to said operation bit section code for said operation means;
b) said concurrent means further comprises:
   1) means for concurrently performing any conditional matching operations on sub-register level within each said enabled memory element;
   2) means for concurrently performing any conditional content moving operations on sub-register level (A) within each said enabled memory element or (B) between each said enabled memory element and corresponding said neighboring memory element; and
   3) means for concurrently performing any conditional adding operations on sub-register level within each said enabled memory element; and
   4) means for concurrently performing conditional general arithmetic operations within each enabled memory element.

189 (New) An apparatus of Claim 125, further comprising:
a) each said memory element further comprises:
   1) said instruction input further comprising:
      A) an operation bit section code; and

B) an operand bit section code;
2) said operand selecting means further comprising means for selecting the bit section of said operand according to said operand bit section code; and
3) operation selecting means for selecting the bit section of said operation register according to said operation bit section code for said operation means;

b) said concurrent means further comprises:
1) means for concurrently performing any conditional logic operations on sub-register level within each said enabled memory element;
1) means for concurrently performing any conditional bitwise logic operations on sub-register level within each said enabled memory element;
2) means for concurrently performing any conditional content moving operations on sub-register level (A) within each said enabled memory element or (B) between each said enabled memory element and corresponding said neighboring memory element;
3) means for concurrently performing any conditional addition/subtraction arithmetic operations on any sub-register level within each said enabled memory element; and
4) means for concurrently performing any conditional general arithmetic operations within each said enabled memory element.

190 (New) An apparatus of Claim 189, further comprising an instruction kernel storing predefined said arithmetic steps and predefined logic steps.

191 (New) An apparatus of Claim 123, further comprising:
a) a priority encoder, comprising:
1) a plurality of bit inputs, each of which has a unique address;
2) a no-hit bit output, which is positively asserted only when none of said bit inputs is positively asserted;
3) a priority high bit input; and
4) an address output, which containing either (A) the highest address of said bit inputs which are positively asserted when said priority high bit input is positively asserted, or (B) the lowest address of said bit inputs which are positively asserted when said priority high bit input is negatively asserted; and
b) means for connecting the match bit output of each said memory element to a unique bit input of said priority encoder wherein the element address of each said memory element equals the corresponding bit input address of said priority encoder; and
c) said finding means further comprising:
1) means for finding no said enabled memory elements whose match bit outputs are positively asserted; and
2) means for finding either (A) the highest or (B) the lowest element address of said enabled memory elements whose match bit outputs are positively asserted.

192 (New) Steps for using apparatus of Claim 191 to store and manage arrays, further comprising:

a) steps for storing array either (1) with each array in each memory element or (2) with each array item in each fixed number of neighboring memory elements or (3) with each memory elements contains a fixed number of array items;
b) steps for concurrently defining a new array within an existing array;
c) steps for concurrently performing a same operation on all array items of said array;
d) steps for concurrently finding in said array no array item satisfying a matching requirement;
e) steps for concurrently finding in said array the array item which (1) satisfies a matching requirement, and (2) has the highest index;
f) steps for concurrently finding in said array the array item which (1) satisfies a matching requirement, and (2) has the lowest index;
g) steps for concurrently enumerating in said array the array items each of which satisfies ~~the~~ a matching requirement;
h) steps for concurrently finding local extreme values of said array;
i) steps for finding a global value bound to said array by concurrent steps;
j) steps for finding a global extreme value of said array by concurrent steps;
k) steps for concurrently inserting a new array item anywhere in said array while keeping all data closely packed;
l) steps for concurrently deleting an existing array item anywhere in said array while keeping all data closely packed;
m) steps for concurrently exchanging two existing neighboring array items anywhere in said array while keeping all data closely packed;
n) steps for concurrently sorting said array by concurrent steps, and
o) steps for concurrently inserting a new array item properly into a sorted said array.
p) steps for numerical characterization of said array by concurrent steps;
q) steps for concurrently finding the degree of matching of each ~~of all the~~ array item of said array for a matching requirement;
r) steps for concurrently carrying out a local logic/arithmetic operation involve neighboring array items by concurrent steps;
s) steps for concurrently matching a template against neighboring array items of ~~the~~ said array by concurrent steps;
t) steps for concurrently carrying out certain global logic/arithmetic operations that treat each array item of said array equally by concurrent steps.

193 (New) An apparatus of Claim 191, further comprising:
a) a parallel counter, comprising:
   1) a plurality of bit inputs,
   2) a count output, and
   3) means for concurrently counting said bit inputs which are positively asserted;
b) means for connecting each match bit output of all said memory elements to a unique bit input of said parallel counter; and
c) said finding means further comprising counting means for concurrently counting said enabled memory elements whose match bit outputs are positively asserted.

194 (New) An apparatus comprising:
a) a plurality of memory elements, each of which comprising:

1) at least one register, comprising:
   A) at least one addressable register;
   B) a shared register;
2) an instruction input, comprising:
   A) a X select bit; and
   B) a Y select bit;
3) an enable bit input;
4) execution means for carrying out instructions at said instruction input only when said enable bit input is positively asserted;
5) a unique element address, comprising
   A) a X address; and
   B) a Y address;
6) only when said memory element is enabled, neighboring means for reading the shared register of a neighboring memory element, said neighboring means further comprising:
   A) when (i) said X select bit is negatively asserted, and (ii) said Y select bit is negatively asserted, means for reading the shared register of the memory element (i) whose X address is immediately lower, and (ii) whose Y address is immediately lower;
   B) when (i) said X select bit is positively asserted, and (ii) said Y select bit is negatively asserted, means for reading the shared register of the memory element (i) whose X address is immediately higher, and (ii) whose Y address is immediately lower;
   C) when (i) said X select bit is negatively asserted, and (ii) said Y select bit is positively asserted, means for reading the shared register of the memory element (i) whose X address is immediately lower, and (ii) whose Y address is immediately higher; and
   D) when (i) said X select bit is positively asserted, and (ii) said Y select bit is positively asserted, means for reading the shared register of the memory element (i) whose X address is immediately higher, and (ii) whose Y address is immediately higher;
7) a match bit output;
8) state means for defining states for said memory element; and
9) matching means for positively asserting said match bit output only when said memory element is in a required state and said enable bit input is positively asserted;

b) an input/output control unit, comprising:
   1) an external bus connection, and
   2) communication means for communicating with said external bus;

c) exclusive means for exclusively copying either (1) the content of any said addressable register to said external bus connection, or (2) the content of said external bus connection to any said addressable register;

d) concurrent means for concurrently executing a same instruction in one or a plural of said memory elements, said concurrent means further comprising:
   1) enabling means for concurrently positively asserting said enable bit inputs of all neighboring memory elements whose element addresses form a two-dimensional

pattern by their X addresses and Y addresses, with said two-dimensional pattern being the enabling pattern;
2) instructing means for sending said instruction concurrently to all said memory elements;
3) executing means for concurrently executing said instruction in all enabled memory elements;
4) matching request means for using a required state for matching concurrently at all enabled memory elements; and
5) finding means for concurrently finding all said memory elements whose match bit outputs have been positively asserted; and

h) instruction means for receiving and carrying out instructions at said external bus connection, further comprising:
1) command means for translating the content at said external bus connection into said exclusive means and said concurrent means;
2) result means for presenting the execution result of said command means at said external bus connection.

195 (New) An apparatus of Claim 194, further comprising:
a) a plurality of bit storage elements;
b) means for connecting each enable bit input of all said memory elements from a unique bit storage element; and
c) said enabling means further comprising means for using said bit storage elements to positively assert each corresponding enable bit input of all said memory elements; and
d) means for writing said bit storage elements with a predefined enabling pattern.

196 (New) An apparatus of Claim 195, further comprising means for concurrently copying said match bit output of all memory element to the corresponding bit storage elements, so that the existing enabling pattern is formed by positively asserted match bit output of all memory elements.

197 (New) An apparatus of Claim 194, further comprising:
a) a X range decoder and a Y range decoder, each range decoder comprising:
1) a start address input;
2) an end address input;
3) a plurality of bit outputs, each of which has a unique address; and
4) means for concurrently positively asserting all said bit outputs whose addresses are: (A) no less than the value at said start address input, and (B) no more than the value at said end address input, while negatively asserting all other said bit outputs; and

b) means for connecting each memory element to the logic AND combination of::
1) a bit output from said X range decoder wherein the address of said bit output is same as said X address of said memory element; and
2) a bit output from said Y range decoder wherein the address of said bit output is same as said Y address of said memory element;

c) said enabling means further comprising XY means for using said X range decoder and said Y range decoder to enable all memory elements:
   1) whose X addresses are: (A) no less than a X start address, and (B) no more than a X end address; and
   2) whose Y addresses are: (A) no less than a Y start address, and (B) no more than a Y end address.

198 (New) An apparatus of Claim 194, further comprising:
a) a X general decoder and a Y general decoder, each general decoder comprising:
   1) a start address input;
   2) an end address input;
   3) a carry number input;
   3) a plurality of bit outputs, each of which has a unique address; and
   4) means for concurrently positively asserting all said bit outputs whose addresses are: (A) no less than the value at said start address input, (B) no more than the value at said end address input, and(C) an integer increment of the value at said carry number input starting from the value at said start address input, while negatively asserting all other said bit outputs; and
b) means for connecting each of all the memory elements to the logic AND combination of::
   1) a bit output from said X general decoder wherein the address of said bit output is same as said X address of said memory element; and
   2) a bit output from said Y general decoder wherein the address of said bit output is same as said Y address of said memory element;
c) said enabling means further comprising XY means for using said X general decoder and said Y general decoder to enable all memory elements:
   1) whose X addresses are: (A) no less than a X start address, (B) no more than a X end address, and (C) an integer increment of a X carry number from said X start address; and
   2) whose Y addresses are: (A) no less than a Y start address, (B) no more than a Y end address, and (C) an integer increment of a Y carry number from said Y start address.

199 (New) An apparatus of Claim 194, wherein:
a) each memory element further comprises:
   1) an operation register;
   2) an status register comprising
      A) a status bit; and
      B) a carry bit;
   3) at least one data registers;
   4) said instruction input further comprising:
      A) a datum;
      B) an operand code, encoding for either (i) said datum, or (ii) said shared register, or (iii) the shared register of said neighboring memory element, or (iv) any of said data registers;
      C) an operation code;

D) a comparison code, encoding for either (i) equal, or (ii) unequal, or (iii) greater than, or (iv) less than, or (v) greater than or equal, or (vi) less than or equal, or (vii) any; and
E) a status code bit;
F) a carry code bit; and
G) a logic code;

5) operand selecting means for selecting an operand according to said operand code;
6) an adder, comprising:
A) a first input;
B) a second input;
C) a carry bit input; and
D) a sum output and a carry bit output, which hold the sum of adding said carry bit input, said first input, and said second input;
7) means for connecting:
A) said first input of said adder from said operation register;
B) said second input of said adder from said operand; and
C) said sum output of said adder to said operation register;
D) said carry bit input of said adder from said carry bit of said status register; and
E) said carry bit output of said adder to said carry bit of said status register;
8) said execution means further comprising operation means for carrying out said operation specified by said operation code, said operation means further comprising:
A) means for positively asserting said match bit output;
B) means for negatively asserting said match bit output;
C) means for positively asserting said status bit;
D) means for negatively asserting said status bit;
E) means for copying the content of said operand to said operation register;
F) means for copying the content of said operation register to said operand when said operand is either (i) said shared register, or (ii) any of said data registers;
G) means for positively asserting said carry bit of the status register;
H) means for negatively asserting said carry bit of the status register; and
I) means for adding said operand to said operation register; and
9) a value comparator comparing said operand and said operation register, and outputting a comparison result;
10) a logic control unit, comprising:
A) means for positively asserting a comparison logic bit only when said comparison result meets said comparison code;
B) means for positively asserting a status logic bit only when said status bit and said status code bit are identically asserted; and
C) means for positively asserting a carry logic bit only when said carry bit and said carry code bit are identically asserted; and
D) condition means for positively asserting a bit output only when the logic combination of (i) said comparison logic bit and (ii) said status logic bit and (ii) said carry logic bit meets said logic code;
9) said enabling means further comprising means for enabling said operation means only when said bit output of said logic control unit is positively asserted; and

b) said concurrent means further comprises:
   1) means for concurrently performing any conditional matching operations within each said enabled memory element;
   2) means for concurrently performing any content moving operations either (A) within each said enabled memory element or (B) between each said enabled memory element and corresponding said neighboring memory element; and
   3) means for concurrently performing any conditional adding operations within each said enabled memory element.

200 (New) An apparatus of Claim 199, wherein:
a) each said memory element further comprises:
   1) said instruction input further comprising:
      A) an operation bit section code; and
      B) an operand bit section code;
   2) said operand selecting means further comprising means for selecting the bit section of said operand according to said operand bit section code; and
   3) operation selecting means for selecting the bit section of said operation register according to said operation bit section code for said operation means;
b) said concurrent means further comprises:
   1) means for concurrently performing any conditional matching operations on sub-register level within each said enabled memory element;
   2) means for concurrently performing any conditional content moving operations on sub-register level (A) within each said enabled memory element or (B) between each said enabled memory element and corresponding said neighboring memory element;
   3) means for concurrently performing any conditional adding operations on sub-register level within each said enabled memory element; and
   4) means for concurrently performing conditional general arithmetic operations within each enabled memory element.

201 An apparatus of Claim 199, wherein:
a) each said memory element further comprising:
   1) said adder further comprising:
      A) an AND output; which holds bitwise AND combination of said first input and said second input;
      B) an OR output; which holds bitwise OR combination of said first input and said second input;
      C) a XOR output; which holds bitwise XOR combination of said first input and said second input; and
      D) a NOT output; which holds bitwise NOT of said second input; and
   2) operation selecting means for copying an output of said adder to said operation register according to said operation code;
   3) said operation means further comprising:
      A) means for outputting bitwise NOT of said operand;
      B) means for subtracting said operand from said operation register;
      C) means for masking said operation register by bitwise AND with said operand;

D) means for masking said operation register by bitwise AND with the bitwise NOT of said operand;
E) means for masking said operation register by bitwise OR with said operand;
F) means for masking said operation register by bitwise OR with the bitwise NOT of said operand;
G) means for masking said operation register by bitwise XOR with said operand;
H) means for masking said operation register by bitwise XOR with the bitwise NOT of said operand;

b) said concurrent means further comprising:
1) means for concurrently performing conditional bitwise logic operations within each enabled memory element;
2) means for concurrently performing conditional addition/subtraction arithmetic operations within each enabled memory element; and
3) means for concurrently performing conditional general arithmetic operations within each enabled memory element.

202 (New) An apparatus of Claim 199, further comprising an instruction kernel storing predefined steps of said logic means and said arithmetic means.

203 (New) An apparatus of Claim 199, further comprising:
a) a priority encoder, comprising:
1) a plurality of bit inputs, each of which corresponds to a unique address;
2) a no-hit bit output, which is positively asserted only when none of the bit inputs is positively asserted;
3) a priority high bit input; and
4) an address output, which contains either (A) the highest address of said bit inputs which are positively asserted when said priority high bit input is positively asserted, or (B) the lowest address of said bit inputs which are positively asserted when said priority high bit input is negatively asserted;
b) means for connecting each match bit output of all said memory elements to a unique bit input of said priority encoder wherein the element address of each said memory element equals the corresponding bit input address of said priority encoder; and
c) said finding means further comprising:
1) means for finding no said enabled memory elements whose match bit outputs are positively asserted; and
2) means for finding either (A) the highest or (B) the lowest element address of said enabled memory elements whose match bit outputs are positively asserted.

204 (New) An apparatus of Claim 203, further comprising:
a) a parallel counter, comprising:
1) a plurality of bit inputs,
2) a count output, and
3) means for concurrently counting said bit inputs which are positively asserted;
b) means for connecting each match bit output of all said memory elements to a unique bit input of said parallel counter; and

c) said finding means further comprising counting means for concurrently counting said enabled memory elements whose match bit outputs are positively asserted.

205 (New) Steps for using apparatus of Claim 204 in image processing, further comprising:

a) steps for storing image with (1) data for each pixel in each said memory element and (2) with the pattern of said image defined by enabled memory elements;
b) steps for concurrently defining a new pattern of pixels within an existing pattern;
c) steps for concurrently finding no pixel value in said pattern satisfying a matching requirement;
d) steps for concurrently enumerating the pixels in said pattern each of which satisfies a matching requirement;
e) steps for concurrently counting the pixels in said pattern each of which satisfies a matching requirement;
f) steps for constructing a histogram of said pattern pixel values by concurrent steps;
g) steps for finding statistical characterization of said pattern pixel values by concurrent steps;
h) steps for finding a global value bound to said pattern pixel values by concurrent steps;
i) steps for concurrently finding the local extreme values of said pattern pixel values;
j) steps for concurrently enlarge or shrinking said pattern through its boundary;
k) steps for concurrently ranking said pattern pixels;
l) steps for concurrently finding the degree of matching for a matching requirement in said pattern;
m) steps for concurrently carrying out local image filtering on said pattern;
n) steps for concurrently carrying out local template matching on said pattern; and
o) steps for concurrently detecting edge lines within said pattern.

206 (New) An apparatus comprising:

a) a plurality of memory elements, each of which comprising:
    1) at least one register, further comprising:
        A) at least one addressable register, and
        B) a shared register;
    2) an enable bit input;
    3) an instruction input;
    4) execution means for carrying out instructions at said instruction input only when said enable bit input is positively asserted;
    5) a unique element address;
    6) only when said enable bit input is positively asserted, neighboring means for reading the shared register of the neighboring memory element whose element address is immediately lower;
    7) a match bit output;
    8) state means for defining states for said memory element; and

9) matching means for positively asserting said match bit output only when said memory element is in a required state and said enable bit input is positively asserted;

b) an input/output control unit, comprising:
   1) an external bus connection, and
   2) communication means for communicating with said external bus;

c) exclusive means for exclusively copying either (1) the content of any said addressable register to said external bus connection, or (2) the content of said external bus connection to any said addressable register;

d) concurrent means for concurrently executing a same instruction in one or a plural of said memory elements, said concurrent means further comprising:
   1) enabling means for concurrently positively asserting said enable bit inputs of all said memory elements whose element addresses are within an address range;
   2) instructing means for sending said instruction concurrently to all said memory elements;
   3) executing means for concurrently executing said instruction in all enabled memory elements;
   4) matching request means for using a required state for matching concurrently in each enabled memory element; and
   5) finding means for concurrently finding all said memory elements whose match bit outputs have been positively asserted; and

e) instruction means for receiving and carrying out instructions at said external bus connection, further comprising:
   1) command means for translating the content at said external bus connection into said exclusive means and said concurrent means;
   2) result means for presenting the execution result of said command means at said external bus connection.

207 (New) An equivalent implementation of apparatus of Claim 206, wherein said neighboring means of each said memory element consisting means for reading the shared register of the neighboring memory element whose element address is immediately higher instead lower;.

208 (New) An apparatus of Claim 206, further comprising:

a) a range decoder, comprising:
   1) a start address input;
   2) an end address input;
   3) a plurality of bit outputs, each of which has a unique address; and
   4) means for concurrently positively asserting all said bit outputs whose addresses are: (A) no less than the value at said start address input, and (B) no more than the value at said end address input, while negatively asserting all other said bit outputs;

b) means for connecting each said memory element to a unique bit output of said range decoder wherein the element address of each said memory element equals the corresponding bit output address of said range decoder; and

c) said enabling means further comprising means for using said range decoder to enable all said memory elements.

209 (New) An apparatus of Claim 206, wherein:
a) each said memory element further comprising:
   1) only one addressable register;
   2) said shared register further comprising a match bit;
   3) said instruction input further comprising:
      A) a datum; and
      B) a self bit;
   4) an equal comparator, comparing said datum and said addressable register, and positively asserting an bit output only when said datum and said addressable register have same value;
   5) asserting means for asserting said match bit when said enabled bit input is positively asserted, said asserting means further comprising:
      A) when said self bit is positively asserted, positively asserting said matching bit only when said bit output of said equal/unequal comparator is positively asserted; or
      B) when said self bit is negatively asserted, positively asserting said match bit only when (A) said bit output of said equal comparator is passively asserted, and (B) the match bit of said neighboring memory element is positively asserted; and
   6) said matching means further comprising means for positively asserting said match bit output only when said match bit is positively asserted; and
b) said concurrent means further comprising:
   1) means for finding equal/unequal match between (A) a datum and (B) the content of said addressable register of each said enabled memory element; and
   2) means for finding any equal/unequal match between (A) a stream of datum and (B) the combined content of said addressable registers of enabled neighboring memory elements.

210 (New) An apparatus of Claim 209, wherein:
a) each said memory element further comprising:
   1) said instruction input further comprising a mask;
   2) means for masking the content of said addressable register with said mask; and
   3) means for comparing said masked content of said addressable register with said datum in said equal/unequal comparator; and
b) said concurrent means further comprising:
   1) means for concurrently finding equal/unequal match between (A) a datum and (B) masked content of addressable register of each said enabled memory element; and
   2) means for concurrently finding equal/unequal match between (A) a stream of datum and (B) combined masked content of addressable registers of enabled neighboring memory elements;

211 (New) An apparatus of Claim 209, wherein:
a) each said memory element further comprising:

1) said instruction input further comprising a transfer bit; and
2) means for transfer the value of the match bit of said neighboring memory element to said match bit when (A) said self bit is negatively asserted, and (B) said transfer bit is positively asserted; and

b) said concurrent means further comprising means for finding equal/unequal match between (A) a stream of datum which contains unspecified datum and (B) the combined content of addressable registers of all enabled neighboring memory elements.

212 (New) An apparatus of Claim 209, further comprising:

a) a priority encoder, comprising:
1) a plurality of bit inputs, each of which has a unique address;
2) a no-hit bit output, which is positively asserted only when none of said bit inputs is positively asserted;
3) a priority high bit input; and
4) an address output, which contains either (A) the highest address of said bit inputs which are positively asserted when said priority high bit input is positively asserted, or (B) the lowest address of said bit inputs which are positively asserted when said priority high bit input is negatively asserted;

b) means for connecting each match bit output of all said memory elements to a unique bit input of said priority encoder wherein the element address of each said memory element equals the corresponding bit input address of said priority encoder; and

c) said finding means further comprising:
1) means for finding no said enabled memory elements whose match bit outputs are positively asserted; and
2) means for finding either (A) the highest or (B) the lowest element address of said enabled memory elements whose match bit outputs are positively asserted.

213 (New) Steps for using apparatus of Claim 213 to store and manage arrays, further comprising:

a) steps for storing each array item either (1) in each memory element or (2) in each fixed number of neighboring memory elements;
b) steps for concurrently defining an array within an existing array;
c) steps for concurrently performing a same operation on all array items of said array;
d) steps for concurrently finding in said array no array item satisfying an equal/unequal matching requirement;
e) steps for concurrently finding in said array the array item which (1) satisfies an equal/unequal matching requirement, and (2) has the highest index; and
f) steps for concurrently enumerating in said array the array items each of which satisfies an equal/unequal matching requirement.

214 (New) An apparatus of Claim 212, further comprising:

a) a parallel counter, comprising:
1) a plurality of bit inputs,
2) a count output, and
3) means for concurrently counting said bit inputs which are positively asserted;

b) means for connecting each match bit output of all said memory elements to a unique bit input of said parallel counter; and
c) said finding means further comprising counting means for concurrently counting said enabled memory elements whose match bit outputs are positively asserted.

215 (New) Steps for using apparatus of Claim 213 to store and manage arrays, further comprising:
a) steps for storing each array item either (1) in each memory element or (2) in each fixed number of neighboring memory elements;
b) steps for concurrently defining an array within an existing array;
c) steps for concurrently performing a same operation on all array items of said array;
d) steps for concurrently finding in said array no array item satisfying an equal/unequal matching requirement;
e) steps for concurrently finding in said array the array item which (1) satisfies an equal/unequal matching requirement, and (2) has the highest index;
f) steps for concurrently enumerating in said array the array items each of which satisfies an equal/unequal matching requirement; and
g) steps for concurrently counting in said array the array items each of which satisfies an equal/unequal matching requirement;